

# MAX30100

## Pulse Oximeter and Heart-Rate Sensor IC for Wearable Health

### General Description

The MAX30100 is an integrated pulse oximetry and heart-rate monitor sensor solution. It combines two LEDs, a photodetector, optimized optics, and low-noise analog signal processing to detect pulse oximetry and heart-rate signals.

The MAX30100 operates from 1.8V and 3.3V power supplies and can be powered down through software with negligible standby current, permitting the power supply to remain connected at all times.

### Applications

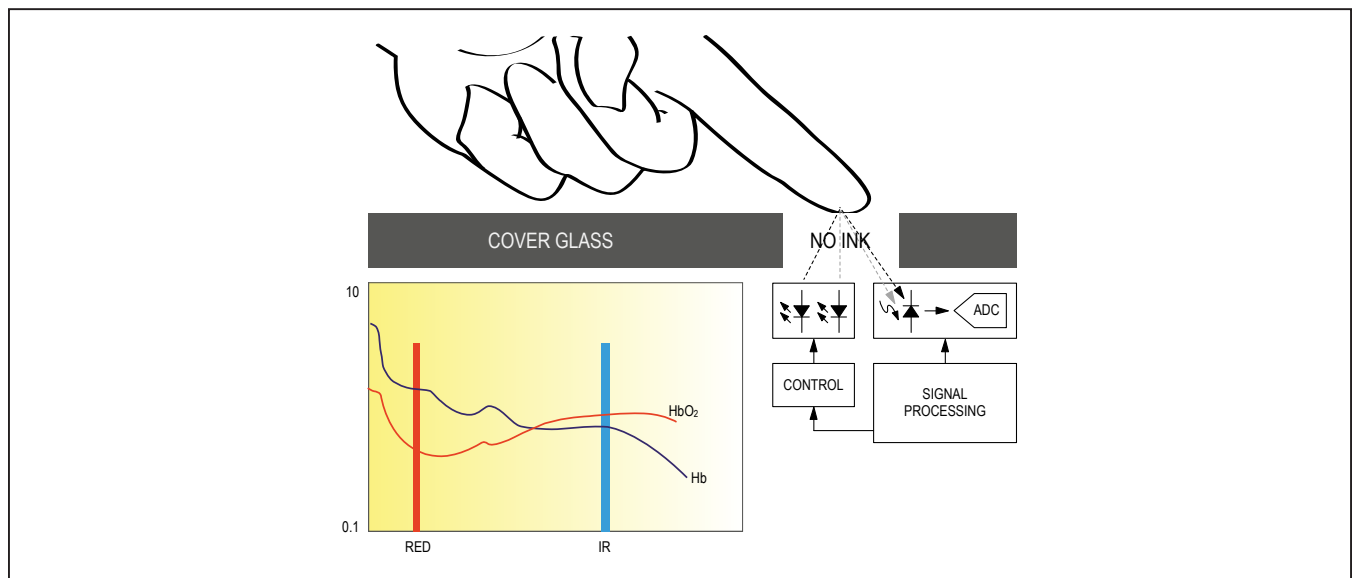
- Wearable Devices
- Fitness Assistant Devices
- Medical Monitoring Devices

### Benefits and Features

- Complete Pulse Oximeter and Heart-Rate Sensor Solution Simplifies Design
  - Integrated LEDs, Photo Sensor, and High-Performance Analog Front -End
  - Tiny 5.6mm x 2.8mm x 1.2mm 14-Pin Optically Enhanced System-in-Package
- Ultra-Low-Power Operation Increases Battery Life for Wearable Devices
  - Programmable Sample Rate and LED Current for Power Savings
  - Ultra-Low Shutdown Current (0.7 $\mu$ A, typ)
- Advanced Functionality Improves Measurement Performance
  - High SNR Provides Robust Motion Artifact Resilience
  - Integrated Ambient Light Cancellation
  - High Sample Rate Capability
  - Fast Data Output Capability

**Ordering Information** appears at end of data sheet.

### System Block Diagram



**Absolute Maximum Ratings**

V <sub>DD</sub> to GND .....	-0.3V to +2.2V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)
GND to PGND .....	-0.3V to +0.3V	OESIP (derate 5.8mW/°C above +70°C) .....
x_DRV, x_LED+ to PGND .....	-0.3V to +6.0V	464mW
All Other Pins to GND .....	-0.3V to +6.0V	Operating Temperature Range .....
Output Short-Circuit Current Duration .....	Continuous	-40°C to +85°C
Continuous Input Current into Any Terminal .....	±20mA	Soldering Temperature (reflow) .....
		+260°C
		Storage Temperature Range .....
		-40°C to +105°C

**Package Thermal Characteristics (Note 1)**

OESIP

Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ) .....	150°C/W
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ) .....	170°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

**Electrical Characteristics**

(V<sub>DD</sub> = 1.8V, V<sub>IR\_LED+</sub> = V<sub>R\_LED+</sub> = 3.3V, T<sub>A</sub> = +25°C, min/max are from T<sub>A</sub> = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
Power-Supply Voltage	V <sub>DD</sub>	Guaranteed by RED and IR count tolerance	1.7	1.8	2.0	V
LED Supply Voltage (R_LED+ or IR_LED+ to PGND)	V <sub>LED+</sub>	Guaranteed by PSRR of LED Driver	3.1	3.3	5.0	V
Supply Current	I <sub>DD</sub>	SpO <sub>2</sub> and heart rate modes, PW = 200µs, 50sps		600	1200	µA
		Heart rate only mode, PW = 200µs, 50sps		600	1200	
Supply Current in Shutdown	I <sub>SHDN</sub>	T <sub>A</sub> = +25°C, MODE = 0x80		0.7	10	µA
<b>SENSOR CHARACTERISTICS</b>						
ADC Resolution				14		bits
Red ADC Count (Note 3)	RED <sub>C</sub>	Propriety ATE setup RED_PA = 0x05, LED_PW = 0x00, SPO2_SR = 0x07, T <sub>A</sub> = +25°C	23,000	26,000	29,000	Counts
IR ADC Count (Note 3)	IR <sub>C</sub>	Propriety ATE setup IR_PA = 0x09, LED_PW = 0x00, SPO2_SR = 0x07, T <sub>A</sub> = +25°C	23,000	26,000	29,000	Counts
Dark Current Count	DC <sub>C</sub>	RED_PA = IR_PA = 0x00, LED_PW = 0x03, SPO2_SR = 0x01		0	3	Counts
DC Ambient Light Rejection (Note 4)	ALR	Number of ADC counts with finger on sensor under direct sunlight (100K lux) LED_PW = 0x03, SPO2_SR = 0x01	RED LED	0		Counts
			IR LED	0		

**Electrical Characteristics (continued)**(V<sub>DD</sub> = 1.8V, V<sub>IR\_LED+</sub> = V<sub>R\_LED+</sub> = 3.3V, T<sub>A</sub> = +25°C, min/max are from T<sub>A</sub> = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IR ADC Count—PSRR (V <sub>DD</sub> )	PSRR <sub>VDD</sub>	Propriety ATE setup 1.7V < V <sub>DD</sub> < 2.0V, LED_PW = 0x03, SPO2_SR = 0x01, IR_PA = 0x09, IR_PA = 0x05, T <sub>A</sub> = +25°C		0.25	2	%
		Frequency = DC to 100kHz, 100mV <sub>p-p</sub>		10		LSB
RED/IR ADC Count—PSRR (X <sub>LED+</sub> )	PSRR <sub>LED</sub>	Propriety ATE setup 3.1V < X <sub>LED+</sub> < 5V, LED_PW = 0x03, SPO2_SR = 0x01, IR_PA = 0x09, IR_PA = 0x05, T <sub>A</sub> = +25°C		0.05	2	%
		Frequency = DC to 100kHz, 100mV <sub>p-p</sub>		10		LSB
ADC Integration Time	INT	LED_PW = 0x00		200		μs
		LED_PW = 0x03		1600		μs
<b>IR LED CHARACTERISTICS (Note 4)</b>						
LED Peak Wavelength	λ <sub>P</sub>	I <sub>LED</sub> = 20mA, T <sub>A</sub> = +25°C	870	880	900	nm
Full Width at Half Max	Δλ	I <sub>LED</sub> = 20mA, T <sub>A</sub> = +25°C		30		nm
Forward Voltage	V <sub>F</sub>	I <sub>LED</sub> = 20mA, T <sub>A</sub> = +25°C		1.4		V
Radiant Power	P <sub>O</sub>	I <sub>LED</sub> = 20mA, T <sub>A</sub> = +25°C		6.5		mW
<b>RED LED CHARACTERISTICS (Note 4)</b>						
LED Peak Wavelength	λ <sub>P</sub>	I <sub>LED</sub> = 20mA, T <sub>A</sub> = +25°C	650	660	670	nm
Full Width at Half Max	Δλ	I <sub>LED</sub> = 20mA, T <sub>A</sub> = +25°C		20		nm
Forward Voltage	V <sub>F</sub>	I <sub>LED</sub> = 20mA, T <sub>A</sub> = +25°C		2.1		V
Radiant Power	P <sub>O</sub>	I <sub>LED</sub> = 20mA, T <sub>A</sub> = +25°C		9.8		mW
<b>TEMPERATURE SENSOR</b>						
Temperature ADC Acquisition Time	T <sub>T</sub>	T <sub>A</sub> = +25°C		29		ms
Temperature Sensor Accuracy	T <sub>A</sub>	T <sub>A</sub> = +25°C		±1		°C
Temperature Sensor Minimum Range	T <sub>MIN</sub>			-40		°C
Temperature Sensor Maximum Range	T <sub>MAX</sub>			85		°C

**Electrical Characteristics (continued)**(V<sub>DD</sub> = 1.8V, V<sub>IR\_LED+</sub> = V<sub>R\_LED+</sub> = 3.3V, T<sub>A</sub> = +25°C, min/max are from T<sub>A</sub> = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DIGITAL CHARACTERISTICS (SDA, SDA, <math>\overline{\text{INT}}</math>)</b>						
Output Low Voltage SDA, $\overline{\text{INT}}$	V <sub>OL</sub>	I <sub>SINK</sub> = 6mA			0.4	V
I <sup>2</sup> C Input Voltage Low	V <sub>IL_I2C</sub>	SDA, SCL			0.4	V
I <sup>2</sup> C Input Voltage High	V <sub>IH_I2C</sub>	SDA, SCL	1.4			V
Input Hysteresis	V <sub>HYS</sub>	SDA, SCL		200		mV
Input Capacitance	C <sub>IN</sub>	SDA, SCL		10		pF
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 0V, T <sub>A</sub> = +25°C (SDA, SCL, INT)		0.01	1	μA
		V <sub>IN</sub> = 5.5V, T <sub>A</sub> = +25°C (SDA, SCL, INT)		0.01	1	μA
<b>I<sup>2</sup>C TIMING CHARACTERISTICS (SDA, SDA, <math>\overline{\text{INT}}</math>)</b>						
I <sup>2</sup> C Write Address				AE		Hex
I <sup>2</sup> C Read Address				AF		Hex
Serial Clock Frequency	f <sub>SCL</sub>		0		400	kHz
Bus Free Time Between STOP and START Conditions	t <sub>BUF</sub>		1.3			μs
Hold Time (Repeated) START Condition	t <sub>HD,START</sub>		0.6			μs
SCL Pulse-Width Low	t <sub>LOW</sub>		1.3			μs
SCL Pulse-Width High	t <sub>HIGH</sub>		0.6			μs
Setup Time for a Repeated START Condition	t <sub>SU,START</sub>		0.6			μs
Data Hold Time	t <sub>HD,DAT</sub>		0		900	ns
Data Setup Time	t <sub>SU,DAT</sub>		100			ns
Setup Time for STOP Condition	t <sub>SU,STOP</sub>		0.6			μs
Pulse Width of Suppressed Spike	t <sub>SP</sub>		0		50	ns
Bus Capacitance	C <sub>B</sub>				400	pF
SDA and SCL Receiving Rise Time	t <sub>R</sub>		20 + 0.1C <sub>B</sub>		300	ns
SDA and SCL Receiving Fall Time	t <sub>RF</sub>		20 + 0.1C <sub>B</sub>		300	ns
SDA Transmitting Fall Time	t <sub>TF</sub>		20 + 0.1C <sub>B</sub>		300	ns

**Note 2:** All devices are 100% production tested at T<sub>A</sub> = +25°C. Specifications over temperature limits are guaranteed by Maxim Integrated's bench or proprietary automated test equipment (ATE) characterization.

**Note 3:** Specifications are guaranteed by Maxim Integrated's bench characterization and by 100% production test using proprietary ATE setup and conditions.

**Note 4:** For design guidance only. Not production tested.

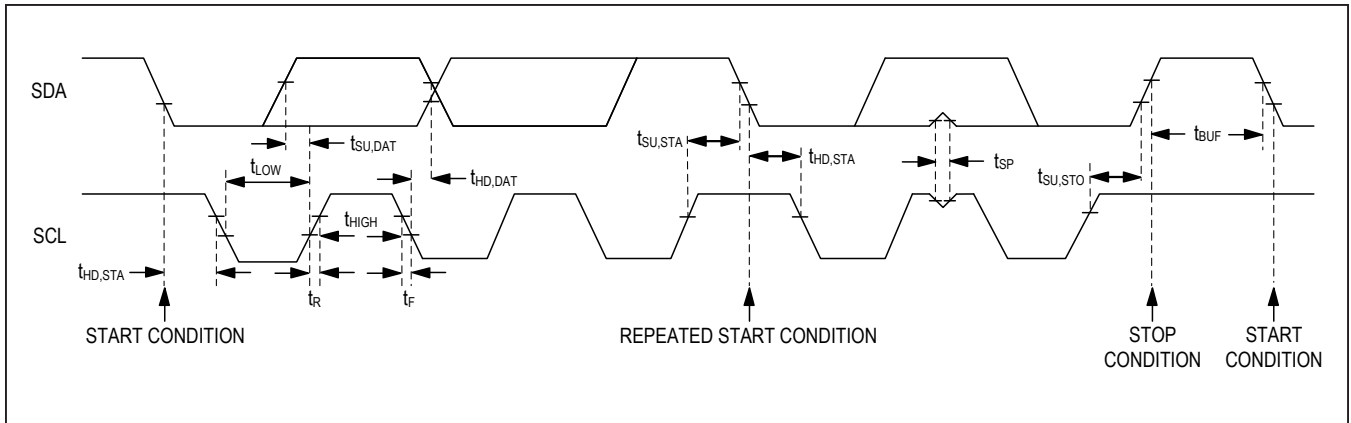
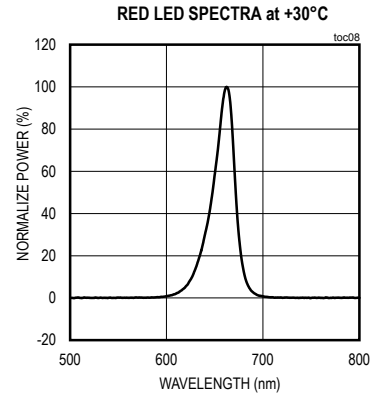
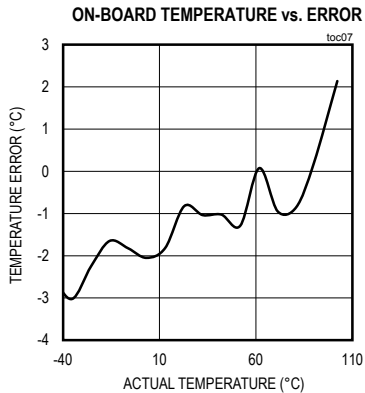
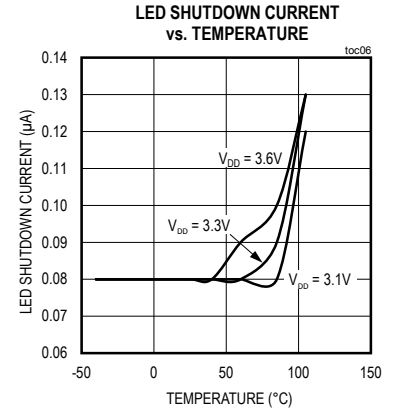
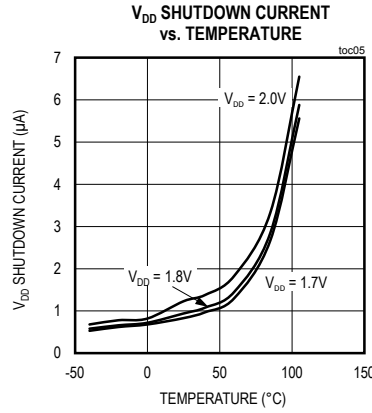
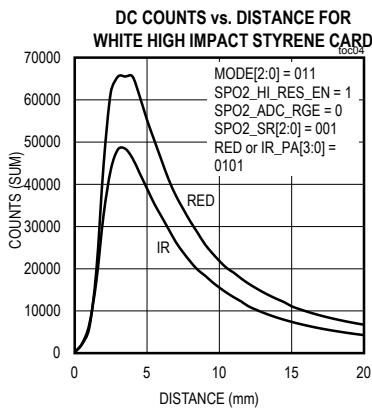
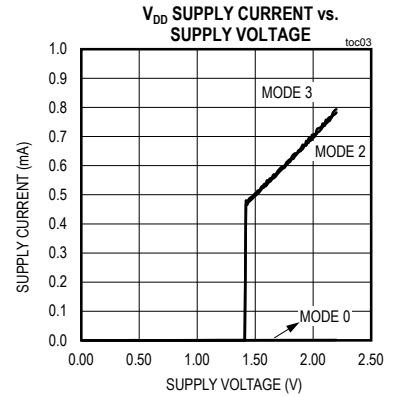
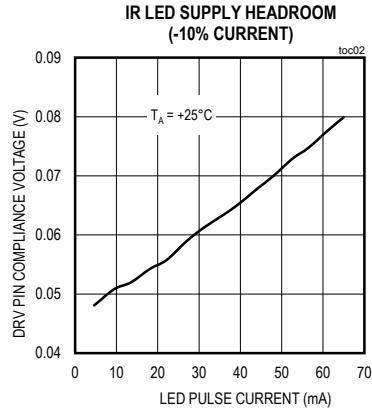
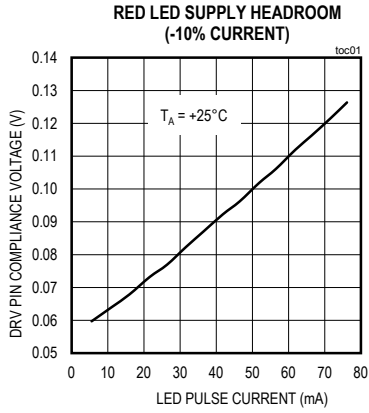


Figure 1. I<sup>2</sup>C-Compatible Interface Timing Diagram

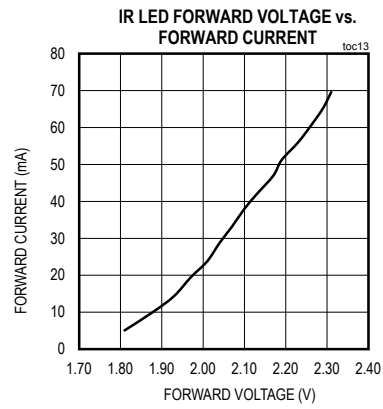
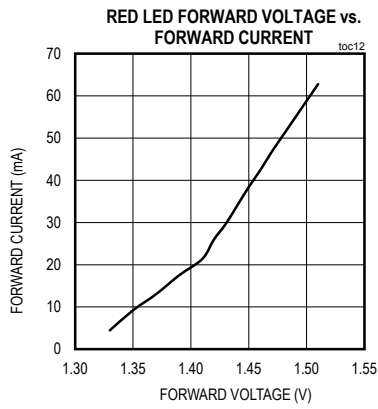
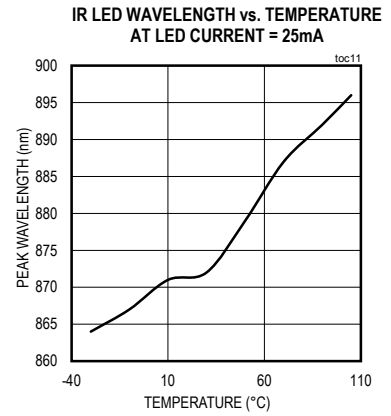
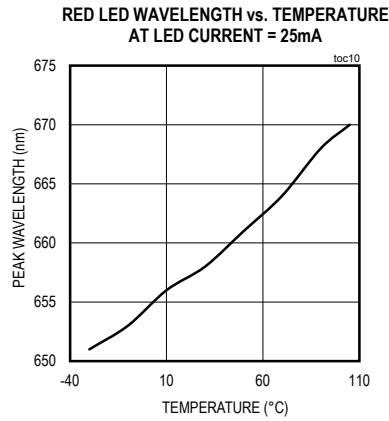
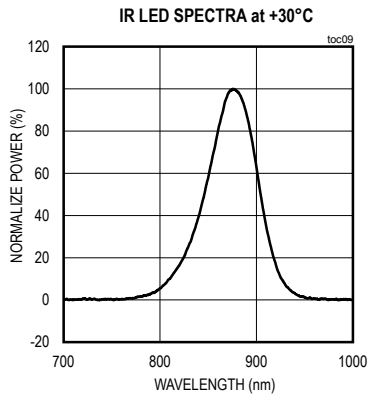
Typical Operating Characteristics

( $V_{DD} = 1.8V$ ,  $V_{IR\_LED+} = V_{R\_LED+} = 3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

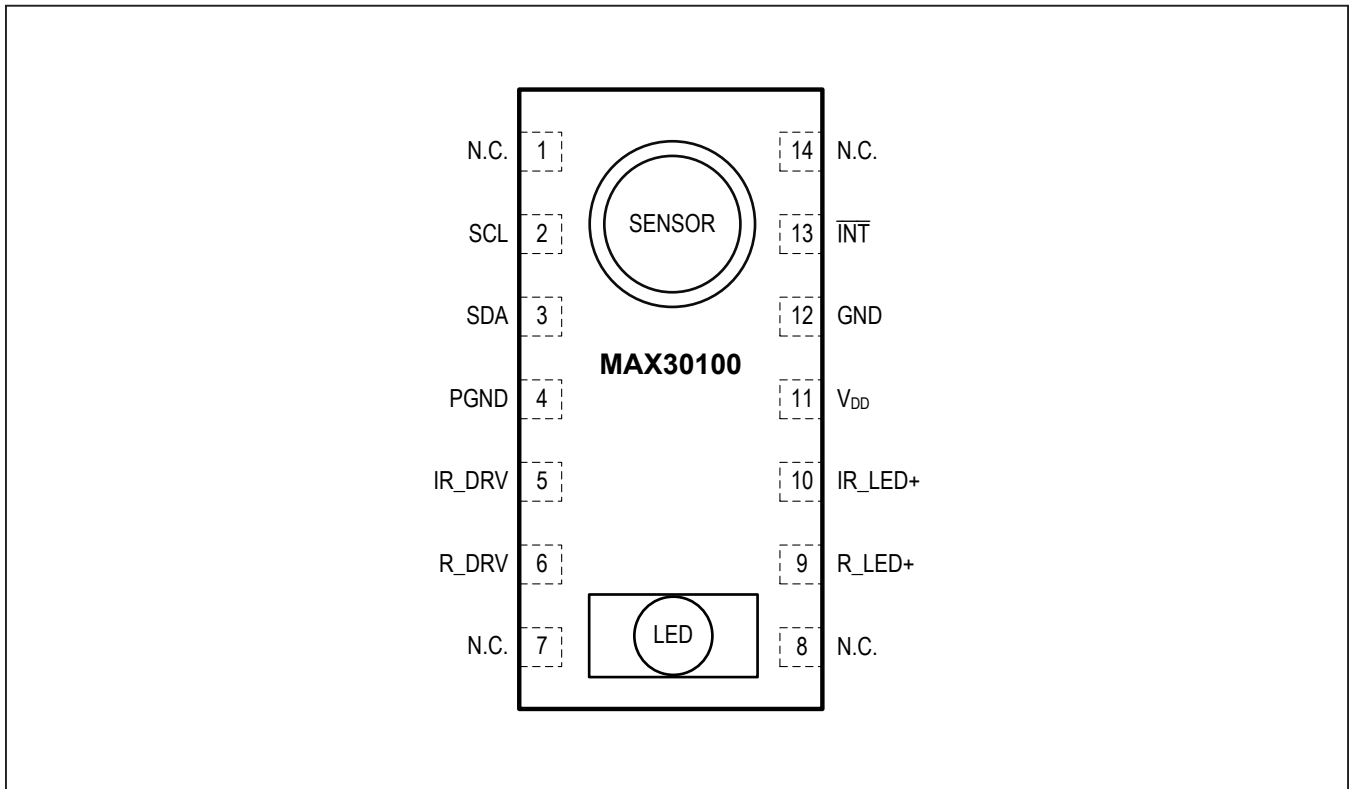


**Typical Operating Characteristics (continued)**

( $V_{DD} = 1.8V$ ,  $V_{IR\_LED+} = V_{R\_LED+} = 3.3V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.)



Pin Configuration

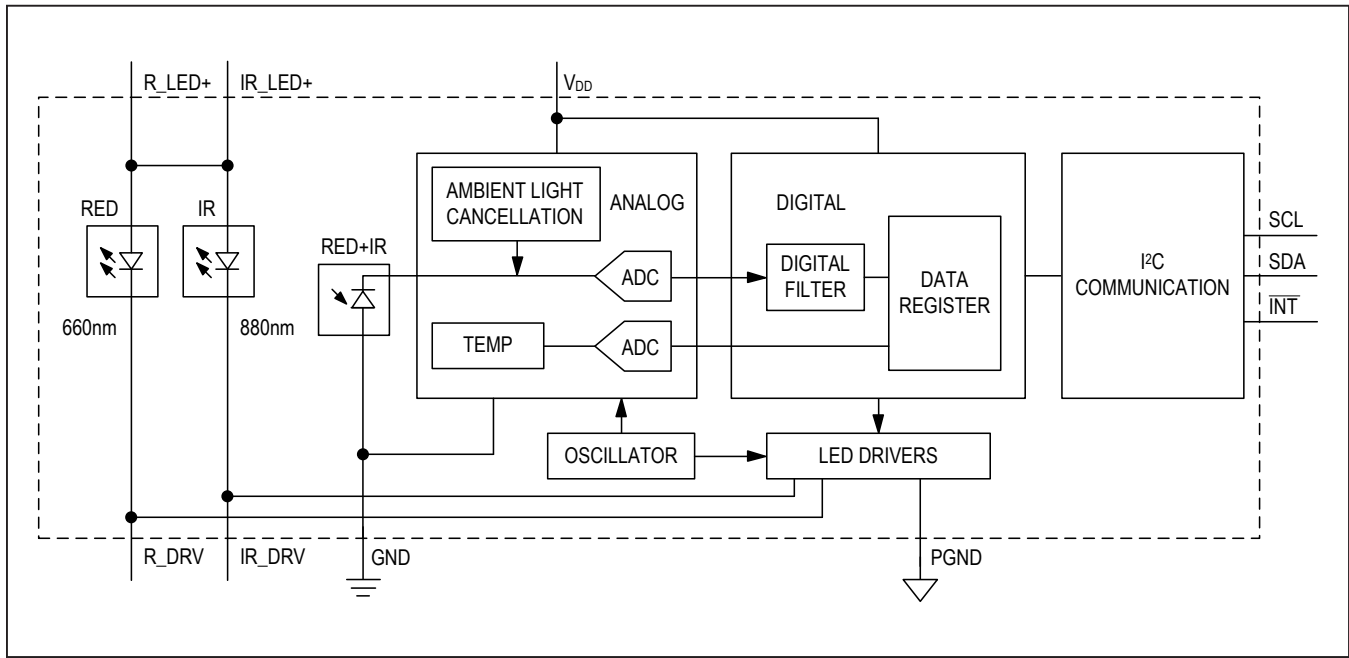


Pin Description

PIN	NAME	FUNCTION
1, 7, 8, 14	N.C.	No Connection. Connect to PCB Pad for Mechanical Stability.
2	SCL	I <sup>2</sup> C Clock Input
3	SDA	I <sup>2</sup> C Clock Data, Bidirectional (Open-Drain)
4	PGND	Power Ground of the LED Driver Blocks
5	IR_DRV	IR LED Cathode and LED Driver Connection Point. Leave floating in circuit.
6	R_DRV	Red LED Cathode and LED Driver Connection Point. Leave floating in circuit.
9	R_LED+	Power Supply (Anode Connection) for Red LED. Bypass to PGND for best performance. Connected to IR_LED+ internally.
10	IR_LED+	Power Supply (Anode Connection) for IR LED. Bypass to PGND for best performance. Connected to R_LED+ internally.
11	V <sub>DD</sub>	Analog Power Supply Input. Bypass to GND for best performance.
12	GND	Analog Ground
13	INT	Active-Low Interrupt (Open-Drain)



## Functional Diagram



## Detailed Description

The MAX30100 is a complete pulse oximetry and heart-rate sensor system solution designed for the demanding requirements of wearable devices. The MAX30100 provides very small total solution size without sacrificing optical or electrical performance. Minimal external hardware components are needed for integration into a wearable device.

The MAX30100 is fully configurable through software registers, and the digital output data is stored in a 16-deep FIFO within the device. The FIFO allows the MAX30100 to be connected to a microcontroller or microprocessor on a shared bus, where the data is not being read continuously from the device's registers.

### SpO<sub>2</sub> Subsystem

The SpO<sub>2</sub> subsystem in the MAX30100 is composed of ambient light cancellation (ALC), 16-bit sigma delta ADC, and proprietary discrete time filter.

The SpO<sub>2</sub> ADC is a continuous time oversampling sigma delta converter with up to 16-bit resolution. The ADC output data rate can be programmed from 50Hz to 1kHz. The

MAX30100 includes a proprietary discrete time filter to reject 50Hz/60Hz interference and low-frequency residual ambient noise.

### Temperature Sensor

The MAX30100 has an on-chip temperature sensor for (optionally) calibrating the temperature dependence of the SpO<sub>2</sub> subsystem.

The SpO<sub>2</sub> algorithm is relatively insensitive to the wavelength of the IR LED, but the red LED's wavelength is critical to correct interpretation of the data. The temperature sensor data can be used to compensate the SpO<sub>2</sub> error with ambient temperature changes.

### LED Driver

The MAX30100 integrates red and IR LED drivers to drive LED pulses for SpO<sub>2</sub> and HR measurements. The LED current can be programmed from 0mA to 50mA (typical only) with proper supply voltage. The LED pulse width can be programmed from 200μs to 1.6ms to optimize measurement accuracy and power consumption based on use cases.

**Table 1. Register Maps and Descriptions**

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
<b>STATUS</b>											
Interrupt Status	A_FULL	TEMP_RDY	HR_RDY	SPO2_RDY				PWR_RDY	0x00	0X00	R
Interrupt Enable	ENB_A_FULL	ENB_TE_P_RDY	ENB_HR_RDY	ENB_S_O2_RDY					0x01	0X00	R/W
<b>FIFO</b>											
FIFO Write Pointer								FIFO_WR_PTR[3:0]	0x02	0x00	R/W
Over Flow Counter								OVF_COUNTER[3:0]	0x03	0x00	R/W
FIFO Read Pointer								FIFO_RD_PTR[3:0]	0x04	0x00	R/W
FIFO Data Register	FIFO_DATA[7:0]								0x05	0x00	R/W
<b>CONFIGURATION</b>											
Mode Configuration	SHDN	RESET			TEMP_EN			MODE[2:0]	0x06	0x00	R/W
SPO2 Configuration		SPO2_HI_RES_EN	RE-SERVED		SPO2_SR[2:0]			LED_PW[1:0]	0x07	0x00	R/W
RESERVED									0x08	0x00	R/W
LED Configuration	RED_PA[3:0]				IR_PA[3:0]				0x09	0x00	R/W
RESERVED									0x0A – 0x15	0x00	R/W
<b>TEMPERATURE</b>											
Temp_Integer	TINT[7:0]								0x16	0x00	R/W
Temp_Fraction								TFRAC[3:0]	0x17	0x00	R/W
RESERVED									0x8D	0x00	R/W
<b>PART ID</b>											
Revision ID	REV_ID[7:0]								0xFE	0xXX*	R
Part ID	PART_ID[7]								0xFF	0x11	R/W

\*XX denotes any 2-digit hexadecimal number (00 to FF). Contact Maxim Integrated for the Revision ID number assigned for your product.

**Interrupt Status (0x00)**

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
Interrupt Status	A_FULL	TEMP_RDY	HR_RDY	SPO2_RDY				PWR_RDY	0x00	0X00	R

There are 5 interrupts and the functionality of each is exactly the same: pulling the active-low interrupt pin into its low state until the interrupt is cleared.

The interrupts are cleared whenever the interrupt status register is read, or when the register that triggered the interrupt is read. For example, if the SpO<sub>2</sub> sensor triggers an interrupt due to finishing a conversion, reading either the FIFO data register or the interrupt register clears the interrupt pin (which returns to its normal high state), and also clears all the bits in the interrupt status register to zero.

**Bit 7: FIFO Almost Full Flag (A\_FULL)**

In SpO<sub>2</sub> and heart-rate modes, this interrupt triggers when the FIFO write pointer is the same as the FIFO read pointer minus one, which means that the FIFO has only one unwritten space left. If the FIFO is not read within the next conversion time, the FIFO becomes full and future data is lost.

**Bit 6: Temperature Ready Flag (TEMP\_RDY)**

When an internal die temperature conversion is finished, this interrupt is triggered so the processor can read the temperature data registers.

**Bit 5: Heart Rate Data Ready (HR\_RDY)**

In heart rate or SPO<sub>2</sub> mode, this interrupt triggers after every data sample is collected. A heart rate data sample consists of one IR data point only. This bit is automatically cleared when the FIFO data register is read.

**Bit 4: SpO<sub>2</sub> Data Ready (SPO2\_RDY)**

In SpO<sub>2</sub> mode, this interrupt triggers after every data sample is collected. An SpO<sub>2</sub> data sample consists of one IR and one red data points. This bit is automatically cleared when the FIFO data register is read.

**Bit 3: RESERVED**

This bit should be ignored and always be zero in normal operation.

**Bit 2: RESERVED**

This bit should be ignored and always be zero in normal operation.

**Bit 1: RESERVED**

This bit should be ignored and always be zero in normal operation.

**Bit 0: Power Ready Flag (PWR\_RDY)**

On power-up or after a brownout condition, when the supply voltage  $V_{DD}$  transitions from below the UVLO voltage to above the UVLO voltage, a power-ready interrupt is triggered to signal that the IC is powered up and ready to collect data.

**Interrupt Enable (0x01)**

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
Interrupt Enable	ENB_A_FULL	ENB_TE_P_RDY	ENB_HR_RDY	ENB_S_O2_RDY					0x01	0X00	R/W

Each source of hardware interrupt, with the exception of power ready, can be disabled in a software register within the MAX30100 IC. The power-ready interrupt cannot be disabled because the digital state of the MAX30100 is reset upon a brownout condition (low power-supply voltage), and the default state is that all the interrupts are disabled. It is important for the system to know that a brownout condition has occurred, and the data within the device is reset as a result.

When an interrupt enable bit is set to zero, the corresponding interrupt appears as 1 in the interrupt status register, but the  $\overline{\text{INT}}$  pin is not pulled low.

The four unused bits (B3:B0) should always be set to zero (disabled) for normal operation.

**FIFO (0x02–0x05)**

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
FIFO Write Pointer					FIFO_WR_PTR[3:0]				0x02	0x00	R/W
Over Flow Counter					OVF_COUNTER[3:0]				0x03	0x00	R/W
FIFO Read Pointer					FIFO_RD_PTR[3:0]				0x04	0x00	R/W
FIFO Data Register	FIFO_DATA[7:0]								0x05	0x00	R/W

**FIFO Write Pointer**

The FIFO write pointer points to the location where the MAX30100 writes the next sample. This pointer advances for each sample pushed on to the FIFO. It can also be changed through the I<sup>2</sup>C interface when MODE[2:0] is nonzero.

**FIFO Overflow Counter**

When the FIFO is full, samples are not pushed on to the FIFO, samples are lost. OVF\_COUNTER counts the number of samples lost. It saturates at 0xF. When a complete sample is popped from the FIFO (when the read pointer advances), OVF\_COUNTER is reset to zero.

**FIFO Read Pointer**

The FIFO read pointer points to the location from where the processor gets the next sample from the FIFO via the I<sup>2</sup>C interface. This advances each time a sample is popped from the FIFO. The processor can also write to this pointer after reading the samples, which would allow rereading samples from the FIFO if there is a data communication error.

**FIFO Data**

The circular FIFO depth is 16 and can hold up to 16 samples of SpO<sub>2</sub> channel data (Red and IR). The FIFO\_DATA register in the I<sup>2</sup>C register map points to the next sample to be read from the FIFO. FIFO\_RD\_PTR points to this sample. Reading FIFO\_DATA register does not automatically increment the register address; burst reading this register reads the same address over and over. Each sample is 4 bytes of data, so this register has to be read 4 times to get one sample.

The above registers can all be written and read, but in practice, only the FIFO\_RD\_PTR register should be written to in operation. The others are automatically incremented or filled with data by the MAX30100. When starting a new SpO<sub>2</sub>

or heart-rate conversion, it is recommended to first clear the FIFO\_WR\_PTR, OVF\_COUNTER, and FIFO\_RD\_PTR registers to all zeros (0x00) to ensure the FIFO is empty and in a known state. When reading the MAX30100 registers in one burst-read I<sup>2</sup>C transaction, the register address pointer typically increments so that the next byte of data sent is from the next register, etc. The exception to this is the FIFO data register, register 0x05. When reading this register, the address pointer does not increment, but the FIFO\_RD\_PTR does. So the next byte of data sent will represent the next byte of data available in the FIFO.

**Reading from the FIFO**

Normally, reading registers from the I<sup>2</sup>C interface autoincrements the register address pointer, so that all the registers can be read in a burst read without an I<sup>2</sup>C restart event. In the MAX30100, this holds true for all registers except for the FIFO\_DATA register (0x05).

Reading the FIFO\_DATA register does not automatically increment the register address; burst reading this register reads the same address over and over. Each sample is 4 bytes of data, so this register has to be read 4 times to get one sample.

The other exception is 0xFF, reading more bytes after the 0xFF register does not advance the address pointer back to 0x00, and the data read is not meaningful.

**FIFO Data Structure**

The data FIFO consists of a 16-sample memory bank that stores both IR and RED ADC data. Since each sample consists of one IR word and one RED word, there are 4 bytes of data for each sample, and therefore, 64 total bytes of data can be stored in the FIFO. [Figure 2](#) shows the structure of the FIFO graphically.

The FIFO data is left-justified as shown in [Table 1](#); i.e. the MSB bit is always in the bit 15 position regardless of ADC resolution.

Each data sample consists of an IR and a red data word (2 registers), so to read one sample requires 4 I<sup>2</sup>C byte reads in a row. The FIFO read pointer is automatically incremented after each 4-byte sample is read.

In heart-rate only mode, the 3rd and 4th bytes of each sample return zeros, but the basic structure of the FIFO remains the same.

**Write/Read Pointers**

**Table 2. FIFO Data**

ADC RESOLUTION	IR [15]	IR [14]	IR [13]	IR [12]	IR [11]	IR [10]	IR [9]	IR [8]	IR [7]	IR [6]	IR [5]	IR [4]	IR [3]	IR [2]	IR [1]	IR [0]
16-bit																
14-bit																
12-bit																
10-bit																

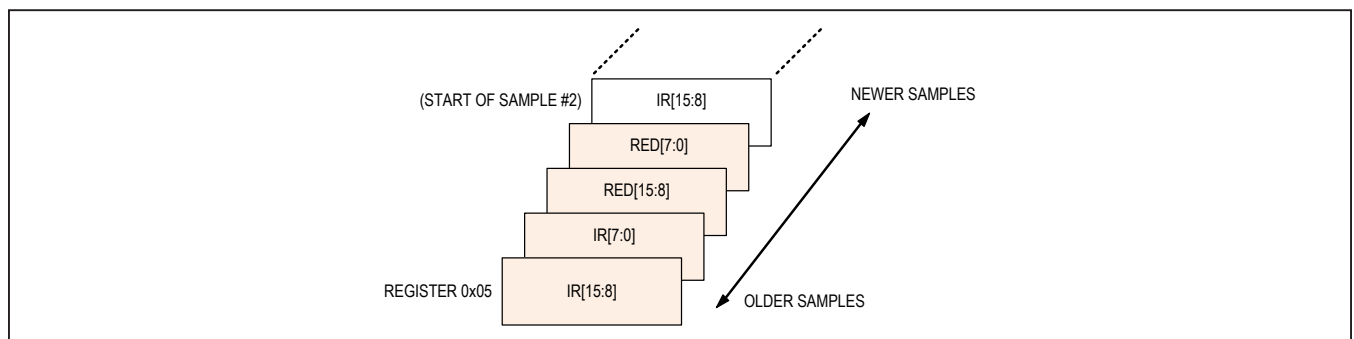


Figure 2. Graphical Representation of the FIFO Data Register

The locations to store new data, and the read pointer for reading data, are used to control the flow of data in the FIFO. The write pointer increments every time a new sample is added to the FIFO. The read pointer is incremented automatically every time a sample is read from the FIFO. To reread a sample from the FIFO, decrement its value by one and read the data register again.

The SpO<sub>2</sub> write/read pointers should be cleared (back to 0x0) upon entering SpO<sub>2</sub> mode or heart-rate mode, so that there is no old data represented in the FIFO. The pointers are not automatically cleared when changing modes, but they are cleared if V<sub>DD</sub> is power cycled so that the V<sub>DD</sub> voltage drops below its UVLO voltage.

#### **Pseudo-Code Example of Reading Data from FIFO**

First transaction: Get the FIFO\_WR\_PTR:

```
START;
Send device address + write mode
Send address of FIFO_WR_PTR;
REPEATED_START;
Send device address + read mode
Read FIFO_WR_PTR;
STOP;
```

The central processor evaluates the number of samples to be read from the FIFO:

```
NUM_AVAILABLE_SAMPLES = FIFO_WR_PTR - FIFO_RD_PTR
(Note: pointer wrap around should be taken into account)
NUM_SAMPLES_TO_READ = < less than or equal to NUM_AVAILABLE_SAMPLES >
```

#### **Second transaction: Read NUM\_SAMPLES\_TO\_READ samples from the FIFO:**

```
START;
Send device address + write mode
Send address of FIFO_DATA;
REPEATED_START;
Send device address + read mode
for (i = 0; i < NUM_SAMPLES_TO_READ; i++) {
Read FIFO_DATA;
Save IR[15:8];
Read FIFO_DATA;
Save IR[7:0];
Read FIFO_DATA;
Save R[15:8];
Read FIFO_DATA;
Save R[7:0];
}
STOP;
```

Third transaction: Write to FIFO\_RD\_PTR register. If the second transaction was successful, FIFO\_RD\_PTR points to the next sample in the FIFO, and this third transaction is not necessary. Otherwise, the processor updates the FIFO\_RD\_PTR appropriately, so that the samples are reread.

```
START;
Send device address + write mode
Send address of FIFO_RD_PTR;
Write FIFO_RD_PTR;
STOP;
```

### Mode Configuration (0x06)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
Mode Configuration	SHDN	RESET			TEMP_EN	MODE[2:0]			0x06	0x00	R/W

#### Bit 7: Shutdown Control (SHDN)

The part can be put into a power-save mode by setting this bit to one. While in power-save mode, all registers retain their values, and write/read operations function as normal. All interrupts are cleared to zero in this mode.

#### Bit 6: Reset Control (RESET)

When the RESET bit is set to one, all configuration, threshold, and data registers are reset to their power-on-state. The only exception is writing both RESET and TEMP\_EN bits to one at the same time since temperature data registers 0x16 and 0x17 are not cleared. The RESET bit is cleared automatically back to zero after the reset sequence is completed.

#### Bit 3: Temperature Enable (TEMP\_EN)

This is a self-clearing bit which, when set, initiates a single temperature reading from the temperature sensor. This bit is cleared automatically back to zero at the conclusion of the temperature reading when the bit is set to one in heart rate or SpO<sub>2</sub> mode.

#### Bits 2:0: Mode Control

These bits set the operating state of the MAX30100. Changing modes does not change any other setting, nor does it erase any previously stored data inside the data registers.

**Table 3. Mode Control**

MODE[2:0]	MODE
000	Unused
001	Reserved (Do not use)
010	HR only enabled
011	SPO <sub>2</sub> enabled
100–111	Unused

**SpO<sub>2</sub> Configuration (0x07)**

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
SpO <sub>2</sub> Configuration		SPO2_HI_RES_EN	Reserved	SPO2_SR[2:0]			LED_PW[1:0]		0x07	0x00	R/W

**Bit 6: SpO<sub>2</sub> High Resolution Enable (SPO2\_HI\_RES\_EN)**

Set this bit high. The SpO<sub>2</sub> ADC resolution is 16-bit with 1.6ms LED pulse width.

**Bit 5: Reserved. Set low (default).****Bit 4:2: SpO<sub>2</sub> Sample Rate Control**

These bits define the effective sampling rate, with one sample consisting of one IR pulse/conversion and one RED pulse/conversion.

The sample rate and pulse width are related, in that the sample rate sets an upper bound on the pulse width time. If the user selects a sample rate that is too high for the selected LED\_PW setting, the highest possible sample rate will instead be programmed into the register.

**Bits 1:0: LED Pulse Width Control**

These bits set the LED pulse width (the IR and RED have the same pulse width), and therefore, indirectly set the integration time of the ADC in each sample. The ADC resolution is directly related to the integration time.

**Table 4. SpO<sub>2</sub> Sample Rate Control**

SPO2_SR[2:0]	SAMPLES (PER SECOND)
000	50
001	100
010	167
011	200
100	400
101	600
110	800
111	1000



**Table 5. LED Pulse Width Control**

LED_PW[1:0]	PULSE WIDTH ( $\mu$ s)	ADC RESOLUTION (BITS)
00	200	13
01	400	14
10	800	15
11	1600	16

**LED Configuration (0x09)**

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
LED Configuration	RED_PA[3:0]				IR_PA[3:0]				0x09	0x00	R/W

**Bits 7:4: Red LED Current Control**

These bits set the current level of the Red LED as in Table 6.

**Bits 3:0: IR LED Current Control**

These bits set the current level of the IR LED as in Table 6.

**Table 6. LED Current Control**

Red_PA[3:0] OR IR_PA[3:0]	TYPICAL LED CURRENT (mA)*
0000	0.0
0001	4.4
0010	7.6
0011	11.0
0100	14.2
0101	17.4
0110	20.8
0111	24.0
1000	27.1
1001	30.6
1010	33.8
1011	37.0
1100	40.2
1101	43.6
1110	46.8
1111	50.0

\*Actual measured LED current for each part can vary widely due to the proprietary trim methodology.

**Temperature Data (0x16–0x17)**

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
Temp_Integer	TINT[7:0]								0x16	0x00	R/W
Temp_Fraction					TFRAC[3:0]				0x17	0x00	R/W

**Temperature Integer**

The on-board temperature ADC output is split into two registers, one to store the integer temperature and one to store the fraction. Both should be read when reading the temperature data, and the following equation shows how to add the two registers together:

$$T_{\text{MEASURED}} = T_{\text{INTEGER}} + T_{\text{FRACTION}}$$

This register stores the integer temperature data in two's complement format, where each bit corresponds to degree Celsius.

**Table 7. Temperature Integer**

REGISTER VALUE (hex)	TEMPERATURE (°C)
0x00	0
0x01	+1
...	...
0x7E	+126
0x7F	+127
0x80	-128
0x81	-127
...	...
0xFE	-2
0xFF	-1

**Temperature Fraction**

This register stores the fractional temperature data in increments of 0.0625°C (1/16<sup>th</sup> of a degree).

If this fractional temperature is paired with a negative integer, it still adds as a positive fractional value (e.g., -128°C + 0.5°C = -127.5°C).

## Applications Information

### Sampling Rate and Performance

The MAX30100 ADC is a 16-bit sigma delta converter. The ADC sampling rate can be configured from 50sps to 1ksp. The maximum sample rate for the ADC depends on the selected pulse width, which in turn, determines the ADC resolution. For instance, if the pulse width is set to 200 $\mu$ s, then the ADC resolution is 13 bits and all sample rates from 50sps to 1ksp are selectable. However, if the pulse width is set to 1600 $\mu$ s, then only sample rates of 100sps and 50sps can be set. The allowed sample rates for both SpO<sub>2</sub> and HR mode are summarized in [Table 8](#) and [Table 9](#).

### Power Considerations

The LEDs in MAX30100 are pulsed with a low duty cycle for power savings, and the pulsed currents can cause ripples in the LED power supply. To ensure these pulses do not translate into optical noise at the LED outputs, the power supply must be designed to handle peak LED current. Ensure that the resistance and inductance from the

power supply (battery, DC/DC converter, or LDO) to the device LED+ pins is much smaller than 1 $\Omega$ , and that there is at least 1 $\mu$ F of power-supply bypass capacitance to a low impedance ground plane. The decoupling capacitor should be located physically as close as possible to the MAX30100 device.

In the heart-rate only mode, the red LED is inactive, and only the IR LED is used to capture optical data and determine the heart rate. This mode allows power savings due to the red LED being off; in addition, the IR\_LED+ power supply can be reduced to save power because the forward voltage of the IR LED is significantly less than that of the red LED.

The average I<sub>DD</sub> and LED current as function of pulse width and sampling rate is summarized in [Table 10](#) to [Table 13](#).

**Table 8. SpO<sub>2</sub> Mode (Allowed Settings)**

SAMPLES (per second)	PULSE WIDTH ( $\mu$ s)			
	200	400	800	1600
50	O	O	O	O
100	O	O	O	O
167	O	O	O	
200	O	O	O	
400	O	O		
600	O			
800	O			
1000	O			
Resolution (bits)	13	14	15	16

**Table 9. Heart-Rate Mode (Allowed Settings)**

SAMPLES (per second)	PULSE WIDTH ( $\mu$ s)			
	200	400	800	1600
50	O	O	O	O
100	O	O	O	O
167	O	O	O	
200	O	O	O	
400	O	O		
600	O	O		
800	O	O		
1000	O	O		
Resolution (bits)	13	14	15	16

**Table 10. SpO<sub>2</sub> Mode: Average IDD  
Current (μA) R\_PA = 0x3, IR\_PA = 0x3**

SAMPLES (per second)	PULSE WIDTH (μs)			
	200	400	800	1600
50	628	650	695	782
100	649	691	776	942
167	678	748	887	
200	692	775	940	
400	779	944		
600	865			
800	952			
1000	1037			

**Table 11. SpO<sub>2</sub> Mode: Average LED  
Current (mA) R\_PA = 0x3, IR\_PA = 0x3**

SAMPLES (per second)	PULSE WIDTH (μs)			
	200	400	800	1600
50	0.667	1.332	2.627	5.172
100	1.26	2.516	4.96	9.766
167	2.076	4.145	8.173	
200	2.491	4.93	9.687	
400	4.898	9.765		
600	7.319			
800	9.756			
1000	12.17			

### Hardware Interrupt

The active-low interrupt pin pulls low when an interrupt is triggered. The pin is open-drain and requires a pullup resistor or current source to an external voltage supply (up to +5V from GND). The interrupt pin is not designed to sink large currents, so the pullup resistor value should be large, such as 4.7kΩ.

The internal FIFO stores up to 16 samples, so that the system processor does not need to read the data after

**Table 12. Heart-Rate Mode: Average IDD  
Current (μA) IR\_PA = 0x3**

SAMPLES (per second)	PULSE WIDTH (μs)			
	200	400	800	1600
50	608	616	633	667
100	617	634	669	740
167	628	658	716	831
200	635	670	739	876
400	671	740	878	
600	707	810		
800	743	881		
1000	779	951		

**Table 13. Heart-Rate Mode: Average LED  
Current (mA) IR\_PA = 0x3**

SAMPLES (per second)	PULSE WIDTH (μs)			
	200	400	800	1600
50	0.256	0.511	1.020	2.040
100	0.512	1.022	2.040	4.077
167	0.854	1.705	3.404	6.795
200	1.023	2.041	4.074	8.130
400	2.042	4.074	8.123	
600	3.054	6.089		
800	4.070	8.109		
1000	5.079	10.11		

every sample. Temperature data may be needed to properly interpret SpO<sub>2</sub> data, but the temperature does not need to be sampled very often—once a second or every few seconds should be sufficient. In heart-rate mode temperature information is not necessary.

**Table 14. Red LED Current Settings vs. LED Temperature Rise**

RED LED CURRENT SETTING	RED LED DUTY CYCLE (% OF LED PULSE WIDTH TO SAMPLE TIME)	ESTIMATED TEMPERATURE RISE (ADD TO TEMPERATURE SENSOR MEASUREMENT) (°C)
0001 (3.1mA)	8	0.1
1111 (35mA)	8	2
0001 (3.1mA)	16	0.3
1111 (35mA)	16	4
0001 (3.1mA)	32	0.6
1111 (35mA)	32	8

**Timing for Measurements and Data Collection**

**Timing in SpO<sub>2</sub> Mode**

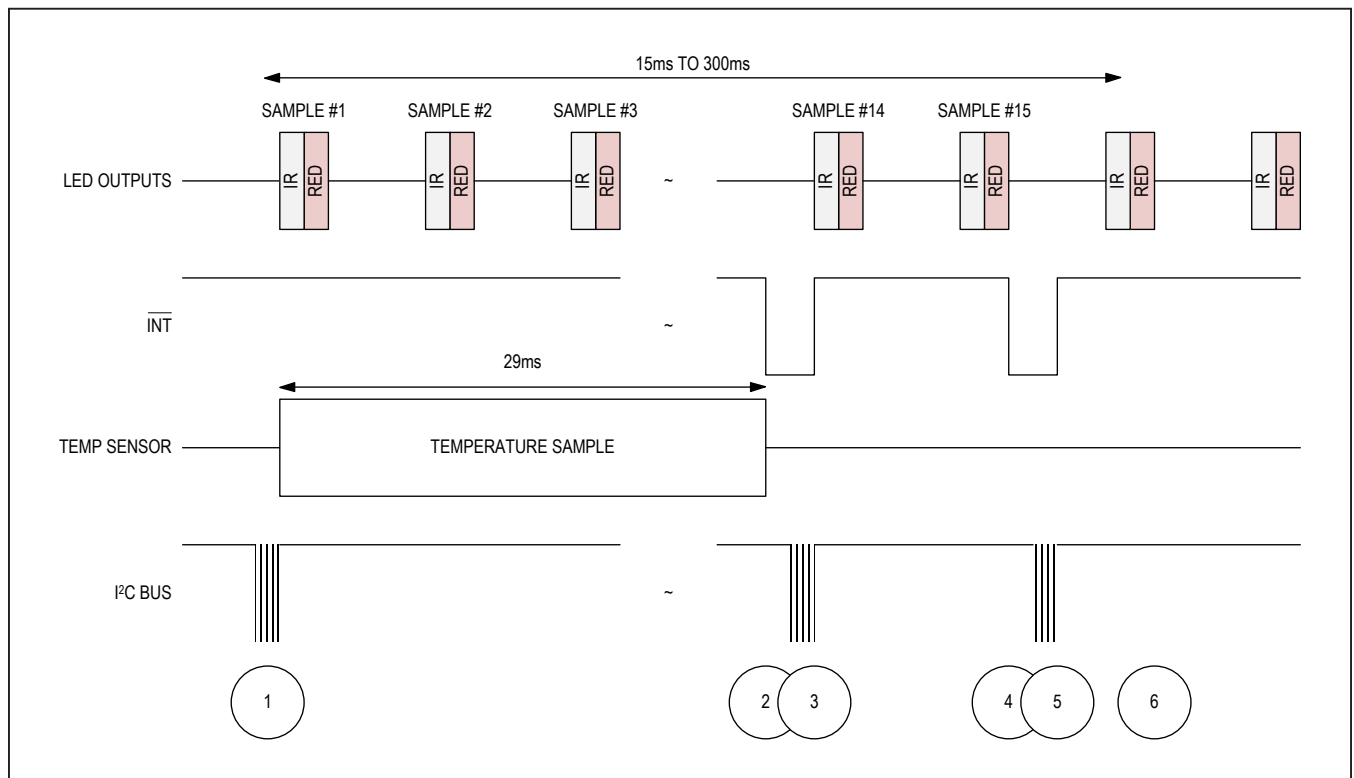


Figure 3. Timing for Data Acquisition and Communication When in SpO<sub>2</sub> Mode

**Table 15. Events Sequence for Figure 3 in SpO<sub>2</sub> Mode**

EVENT	DESCRIPTION	COMMENTS
1	Enter into SpO <sub>2</sub> mode. Initiate a temperature measurement.	I <sup>2</sup> C Write Command Sets MODE[2:0] = 0x03. At the same time, set the TEMP_EN bit to initiate a single temperature measurement. Mask the SPO2_RDY Interrupt.
2	Temperature measurement complete, interrupt generated	TEMP_RDY interrupt triggers, alerting the central processor to read the data.
3	Temp data is read, interrupt cleared	
4	FIFO is almost full, interrupt generated	Interrupt is generated when the FIFO has only one empty space left.
5	FIFO data is read, interrupt cleared	
6	Next sample is stored	New sample is stored at the new read pointer location. Effectively, it is now the first sample in the FIFO.

**Timing in Heart-Rate Mode**

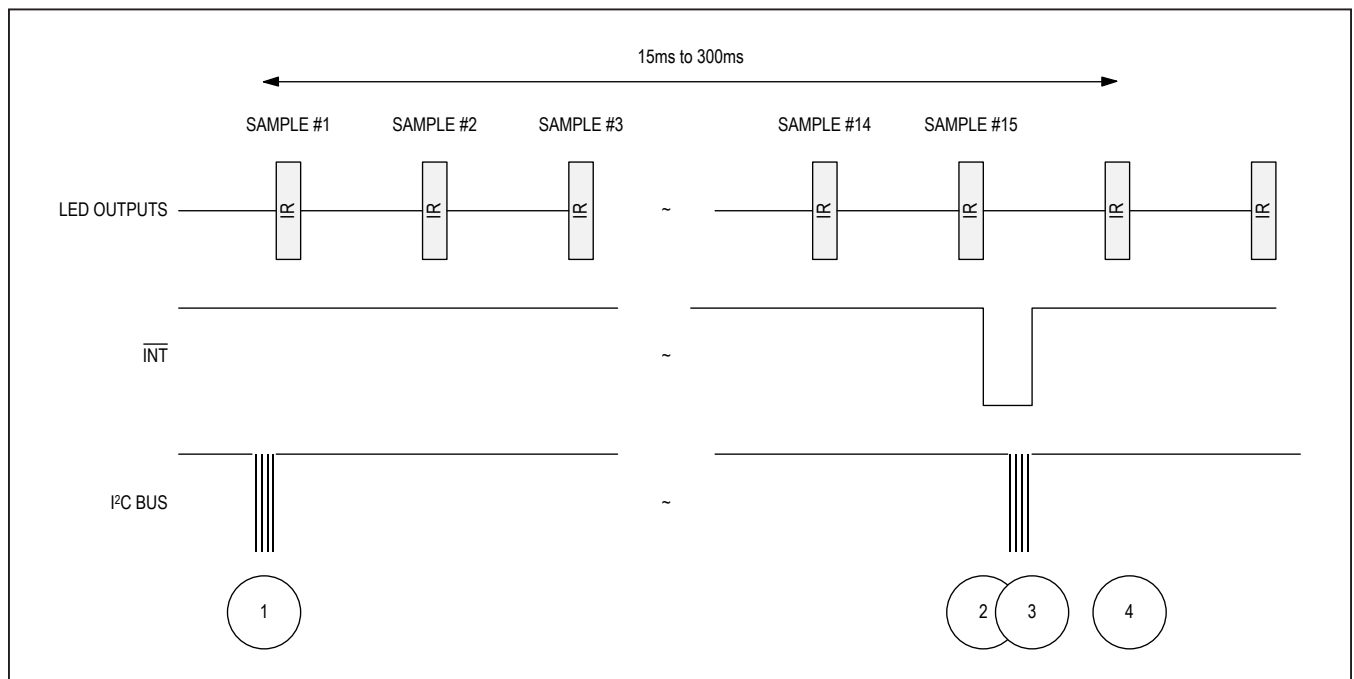


Figure 4. Timing for Data Acquisition and Communication When in Heart Rate Mode

**Table 16. Events Sequence for Figure 4 in Heart-Rate Mode**

EVENT	DESCRIPTION	COMMENTS
1	Enter into heart rate mode	I <sup>2</sup> C Write Command Sets MODE[2:0] = 0x02. Mask the HR_RDY interrupt.
2	FIFO is almost full, interrupt generated	Interrupt is generated when the FIFO has only one empty space left.
3	FIFO data is read, interrupt cleared	
4	Next sample is stored	New sample is stored at the new read pointer location. Effectively, it is now the first sample in the FIFO.

## Power Sequencing and Requirements

### Power-Up Sequencing

Figure 5 shows the recommended power-up sequence for the MAX30100.

It is recommended to power the V<sub>DD</sub> supply first, before the LED power supplies (R\_LED+, IR\_LED+). The interrupt and I<sup>2</sup>C pins can be pulled up to an external voltage even when the power supplies are not powered up.

After the power is established, an interrupt occurs to alert the system that the MAX30100 is ready for operation. Reading the I<sup>2</sup>C interrupt register clears the interrupt, as shown in Figure 5.

### Power-Down Sequencing

The MAX30100 is designed to be tolerant of any power-supply sequencing on power-down.

## I<sup>2</sup>C Interface

The MAX30100 features an I<sup>2</sup>C/SMBus-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX30100 and the master at clock rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX30100 by transmitting the proper slave address followed by data. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX30100 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX30100 transmits the proper slave address followed by a series of nine SCL pulses.

The MAX30100 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output.

### Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals. See the [START and STOP Conditions](#) section.

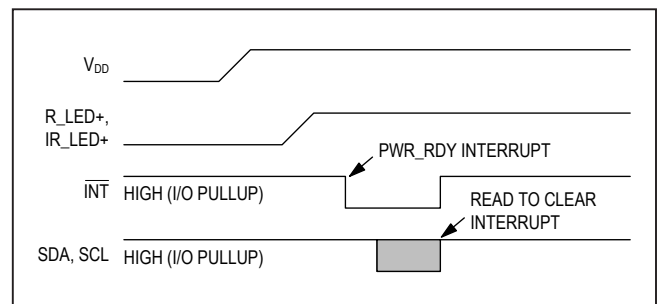


Figure 5. Power-Up Sequence of the Power-Supply Rails

**START and STOP Conditions**

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 6). A START condition from the master signals the beginning of a transmission to the MAX30100. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

**Early STOP Conditions**

The MAX30100 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

**Slave Address**

A bus master initiates communication with a slave device by issuing a START condition followed by the 7-bit slave ID. When idle, the MAX30100 waits for a START condition followed by its slave ID. The serial interface compares each slave ID bit by bit, allowing the interface to power down and disconnect from SCL immediately if an incorrect slave ID is detected. After recognizing a START condition followed by the correct slave ID, the MAX30100 is ready to accept or send data. The LSB of the slave

ID word is the Read/Write (R/W) bit. R/W indicates whether the master is writing to or reading data from the MAX30100. R/W = 0 selects a write condition, R/W = 1 selects a read condition). After receiving the proper slave ID, the MAX30100 issues an ACK by pulling SDA low for one clock cycle.

The MAX30100 slave ID consists of seven fixed bits, B7–B1 (set to 0b1010111). The most significant slave ID bit (B7) is transmitted first, followed by the remaining bits. Table 18 shows the possible slave IDs of the device.

**Acknowledge**

The acknowledge bit (ACK) is a clocked 9th bit that the MAX30100 uses to handshake receipt each byte of data when in write mode (Figure 7). The MAX30100 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master will retry communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX30100 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX30100, followed by a STOP condition.

**Table 17. Slave ID Description**

B7	B6	B5	B4	B3	B2	B1	B0	WRITE ADDRESS	READ ADDRESS
1	0	1	0	1	1	1	R/W	0xAE	0xAF

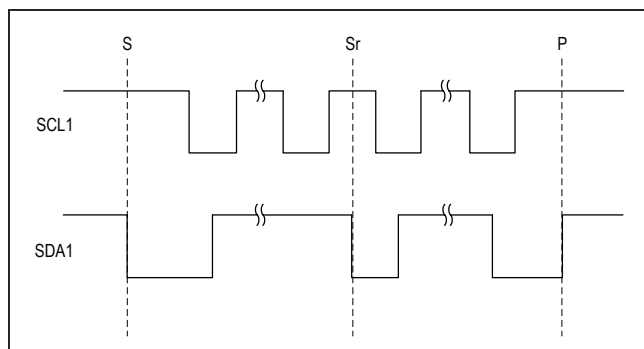


Figure 6. START, STOP, and REPEATED START Conditions

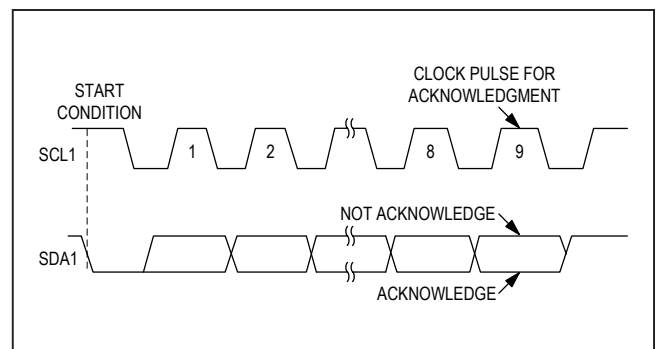


Figure 7. Acknowledge



**Write Data Format**

For the write operation, send the slave ID as the first byte followed by the register address byte and then one or more data bytes. The register address pointer increments automatically after each byte of data received. For example, the entire register bank can be written by at one time. Terminate the data transfer with a STOP condition. The write operation is shown in [Figure 8](#).

The internal register address pointer increments automatically, so writing additional data bytes fill the data registers in order.

**Read Data Format**

For the read operation, two I<sup>2</sup>C operations must be performed. First, the slave ID byte is sent followed by the I<sup>2</sup>C register that you wish to read. Then a REPEATED START (Sr) condition is sent, followed by the read slave ID. The MAX30100 then begins sending data beginning with the register selected in the first operation. The read pointer

increments automatically, so the MAX30100 continues sending data from additional registers in sequential order until a STOP (P) condition is received. The exception to this is the FIFO\_DATA register, at which the read pointer no longer increments when reading additional bytes. To read the next register after FIFO\_DATA, an I<sup>2</sup>C write command is necessary to change the location of the read pointer.

An initial write operation is required to send the read register address.

Data is sent from registers in sequential order, starting from the register selected in the initial I<sup>2</sup>C write operation. If the FIFO\_DATA register is read, the read pointer does not automatically increment, and subsequent bytes of data contain the contents of the FIFO.

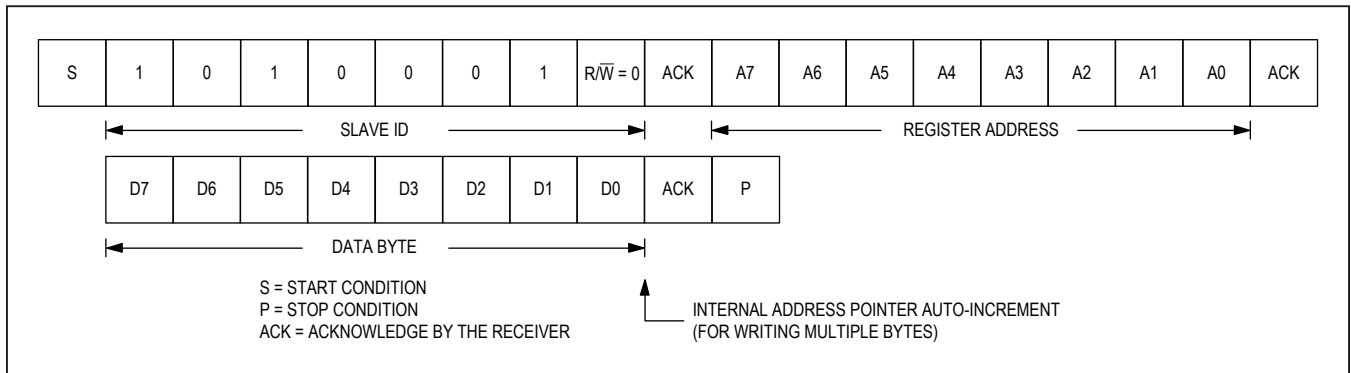


Figure 8. Writing One Data Byte to the MAX30100

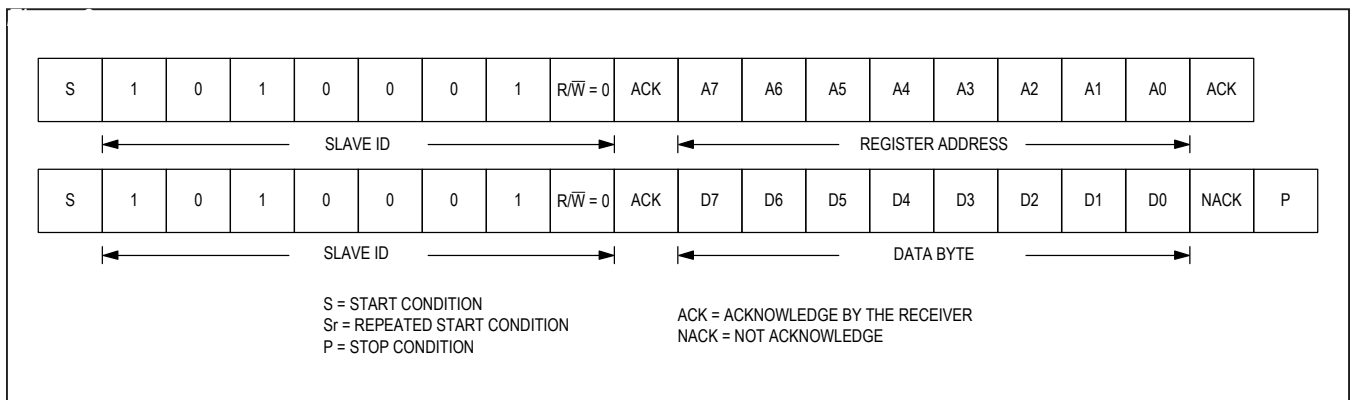


Figure 9. Reading One Byte of Data from the MAX30100

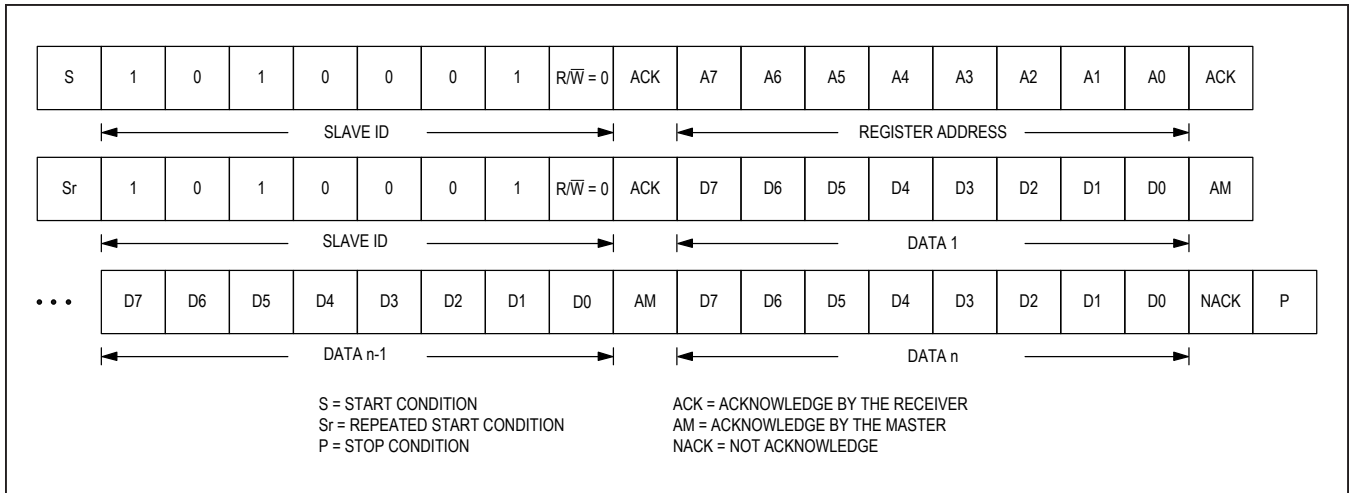
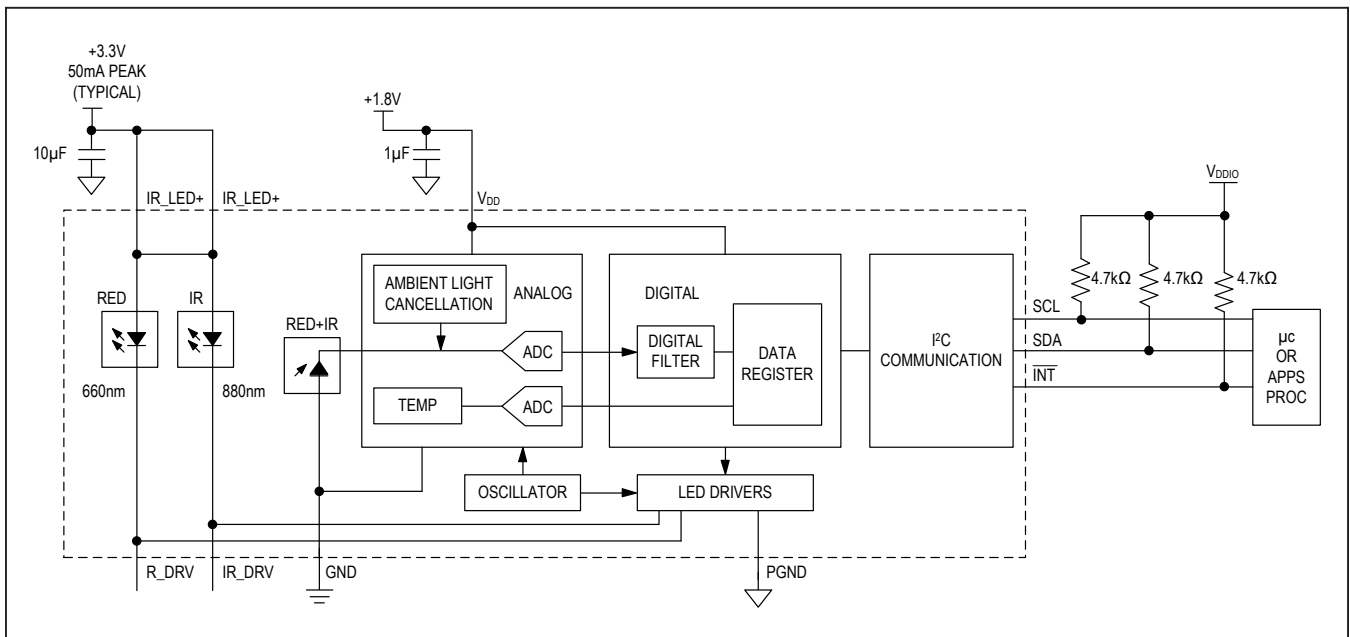


Figure 10. Reading Multiple Bytes of Data from the MAX30100

### Typical Application Circuit



### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX30100EFD+	-40°C to +85°C	14 OESIP (0.8mm pitch)

+Denotes a lead(Pb)-free/RoHS-compliant package.

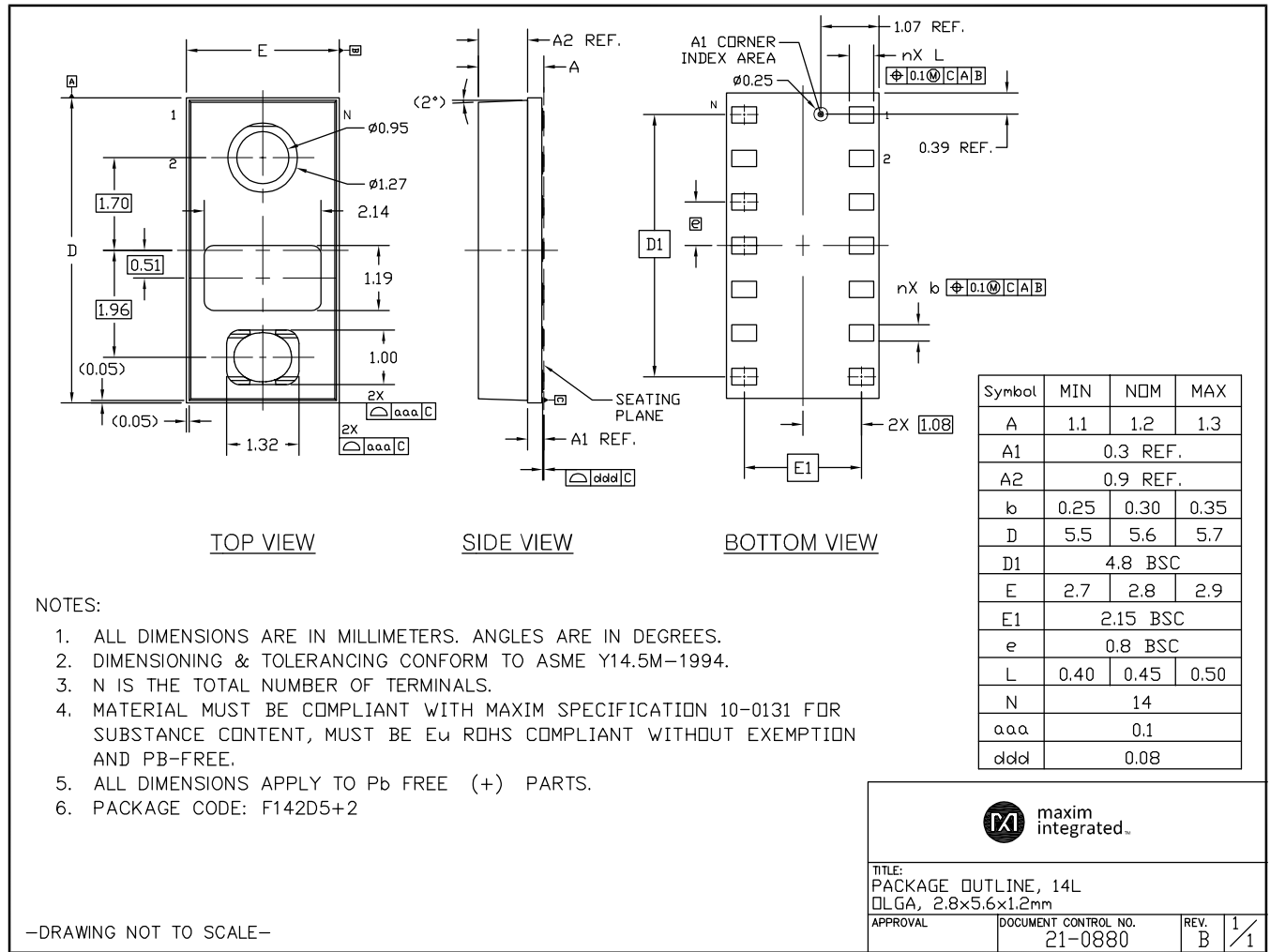
### Chip Information

PROCESS: BiCMOS

Package Information

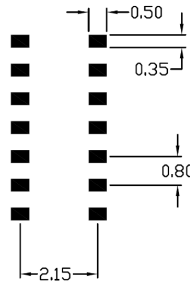
For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 OESIP	F142D5+2	21-0880	90-0461



**Package Information (continued)**

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



NOTES:

1. REFERENCE PKG. OUTLINE: 21-0880.
2. LAND PATTERN COMPLIES TO: IPC7351A.
3. TOLERANCE: +/- 0.02 MM.
4. ALL DIMENSIONS APPLY TO PbFREE (+) PKG. CODE ONLY
5. ALL DIMENSIONS IN MM.

—DRAWING NOT TO SCALE—



This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depend on many factors unknown to Maxim (eg. user's board manufacturing specs), user must determine suitability for use. This document is subject to change without notice. Contact technical support at <http://www.maxim-ic.com/support> for further questions.

TITLE: PACKAGE LAND PATTERN, [F142D5+2] QLGA			
APPROVAL	DOCUMENT CONTROL NO. 90-0461	REV. A	1/1

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/14	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

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