



# NF-05 Specification

Version V1.1.0

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## Content

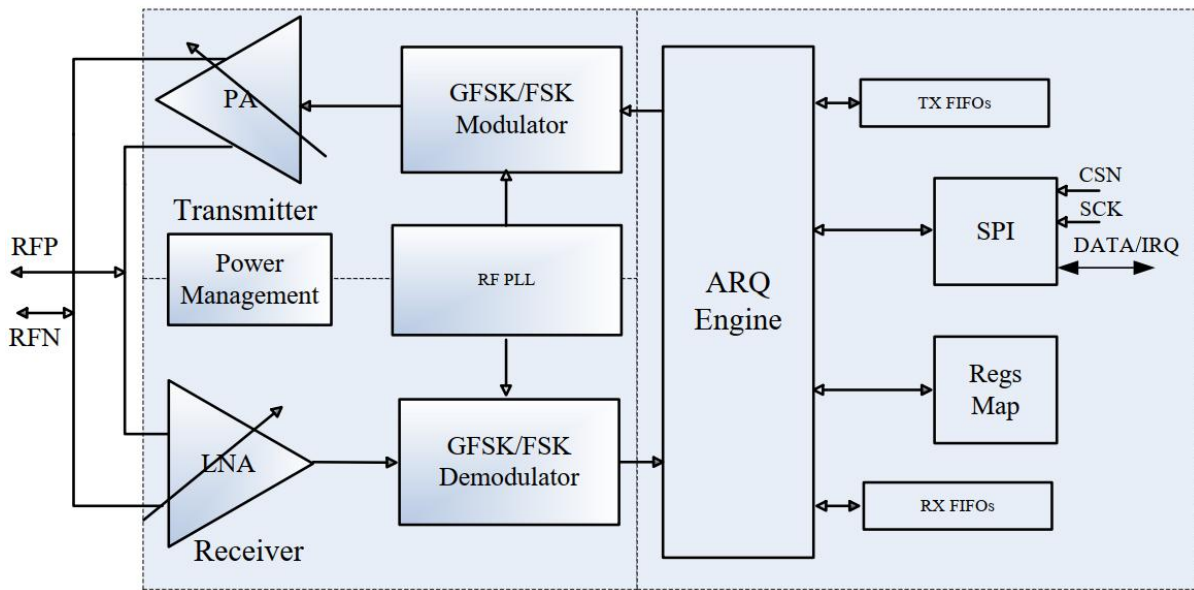
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## 1. Product Overview

NF-05 is a 2.4GHz module developed by Shenzhen Ai-Thinker Technology Co., LTD. The core processor chip Ci24R1 is a high-performance 2.4ghz GFSK wireless transceiver chip, designed for wireless mouse, keyboard, wireless remote control, motion sensing devices, smart power grid, smart home, wireless audio, wireless data transmission and other applications.

NF-05chips have industry-leading low power performance and rf performance, supporting GFSK/FSK protocols. The chip integrates high PSRR LDO and intelligent ARQ baseband protocol engine. The chip has a fast startup time of less than 160uS and ultra-low power consumption of up to 2uA, which can meet the power requirements of various application scenarios. Few peripheral devices greatly reduce the application cost of the system.

NF-05 module rate: 250Kbps, 1Mbps, 2Mbps. Support broadcast, channel selection.



**Figure 1 Main chip architecture diagram**

## 1.1. Characteristic

- Working in 2.4GHz ISM band
- Debug Mode: GFSK/FSK
- Data Rate: 2Mbps/1Mbps/250Kbps
- Ultra-low shutdown power consumption: 2uA
- Fast start selectable recovery time<160uS
- High internal integration PSRR LDO
- Wide power supply voltage range: 2.1-3.6V
- Maximum 10MHz two-wire SPI interface
- Internal integration of intelligent ARQ baseband protocol engine
- The hardware for sending and receiving data is interrupted
- Supports 1bit RSSI output
- Few peripheral devices, reduce the system application cost
- packaged SMD-8

## 2. Main parameters

Table 1 Description of the main parameters

<b>Module Model</b>	NF-05
<b>Package</b>	SMD-8
<b>Size</b>	12.0*18.0*0.8(±0.2)mm
<b>Antenna</b>	On board antenna
<b>Frequency</b>	2400 ~ 2525MHz
<b>Operating temperature</b>	-40 °C ~ 85 °C
<b>Storage temperature</b>	-40 °C ~ 125 °C , < 90%RH
<b>Power supply</b>	Voltage 2.1V ~ 3.6V, Current >100mA
<b>Interface</b>	SPI
<b>IO</b>	3

## 2.1. Static electricity requirements

NF-05 modules are electrostatic sensitive devices. Take special precautions when moving them.



Figure 2 ESD anti-static diagram

## 2.2. Electrical characteristics

Table 2 Electrical characteristics table

Parameter	condition	Min.	Typical	Max.	Unit	
Power supply	VDD	2.1	3.3	3.6	V	
I/O	$V_{IL}/V_{IH}$	-	-0.3/0.75VDD	-	0.25VDD/VDD+0.3	V
	$V_{OL}/V_{OH}$	-	N/0.8VIO	-	0.1VIO/N	V
	$I_{MAX}$	-	-	-	12	mA

## 2.3. 2.4G Rf Performance

Table 3 2.4GHz RF performance table

Description	Typical value	Unit
Working frequency	2400 - 2525	MHz
<b>Output Power</b>		
250Kbps	$8 \pm 2$	dBm
1Mbps	$8 \pm 2$	dBm
2Mbps	$8 \pm 2$	dBm
<b>Receive sensitivity</b>		
250Kbps	$\leq -91$	dBm
1Mbps	$\leq -85$	dBm
2Mbps	$\leq -78$	dBm

## 2.4. Power consumption

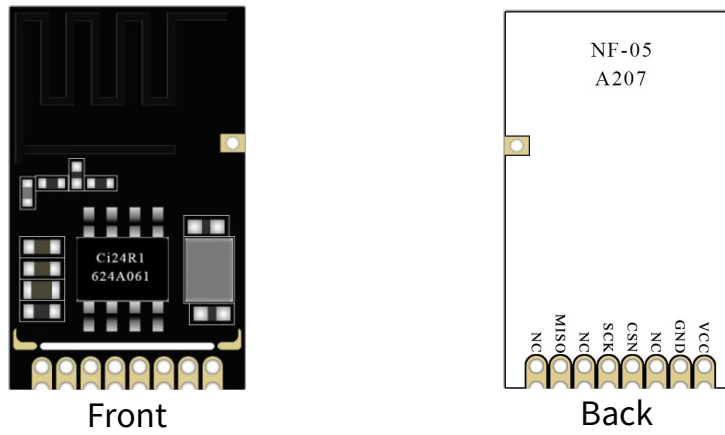
The following power consumption figures are based on a 3.3V power supply at 25°C ambient temperature using current synthesis analysis.

**Table 4 Power consumption table**

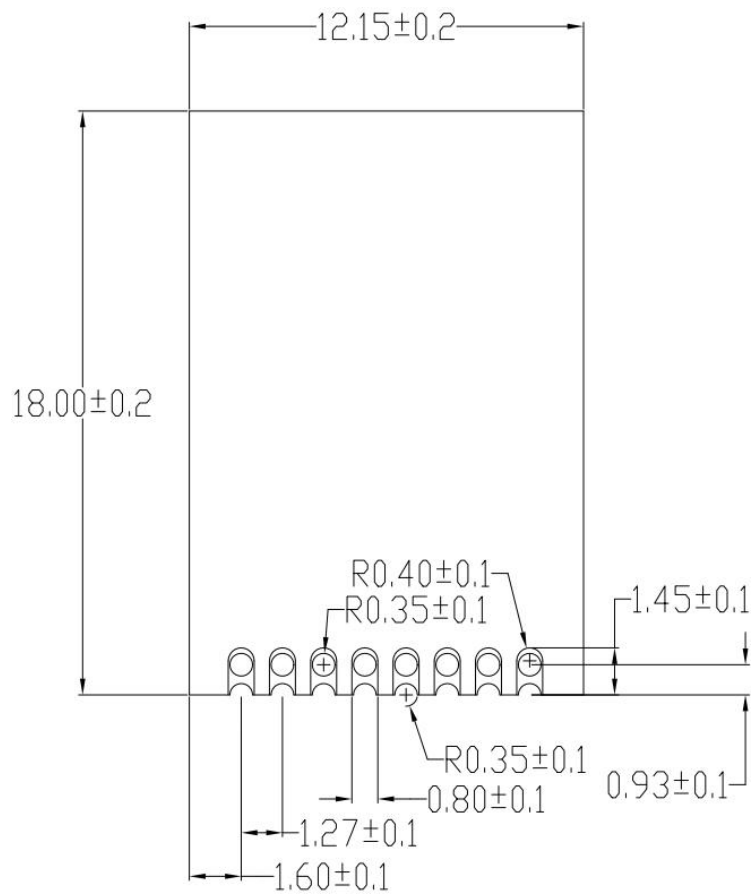
Mode	Min.	AVG	Max.	Unit
TX Power output (11dBm) Mode	-	36.6	-	mA
RX Test Mode	-	16.0	-	mA
Standby mode	-	52.9	-	μA
Off mode	-	1.3	-	μA



### 3. Appearance dimensions



**Figure 3 Module appearance diagram (The rendering is for reference only, the actual product shall prevail)**



**Figure 4 module size diagram**

## 4. Pin Definition

NF-05 module is connected with 8 pins, as shown in pin schematic diagram, pin function definition table is the interface definition.

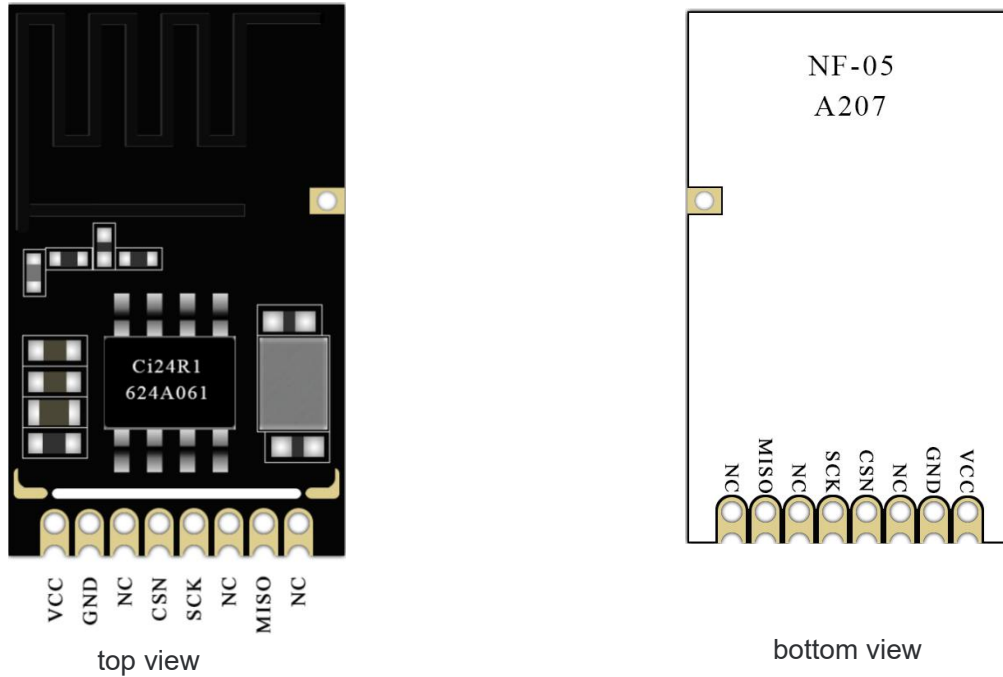


Figure 5 Schematic diagram of module pins (bottom view)

Table 5 Pin function definition table

No.	Name	Function
1	VCC	GND positive pole
2	GND	Power Supply negative pole
3, 6, 8	NC	Empty pin
4	CSN	GCAP-SPI-CS
5	SCK	AP-SPI-CLK
7	MISO	DATA/IQ SPI Data input/output/interrupt signal

## 5. Schematic

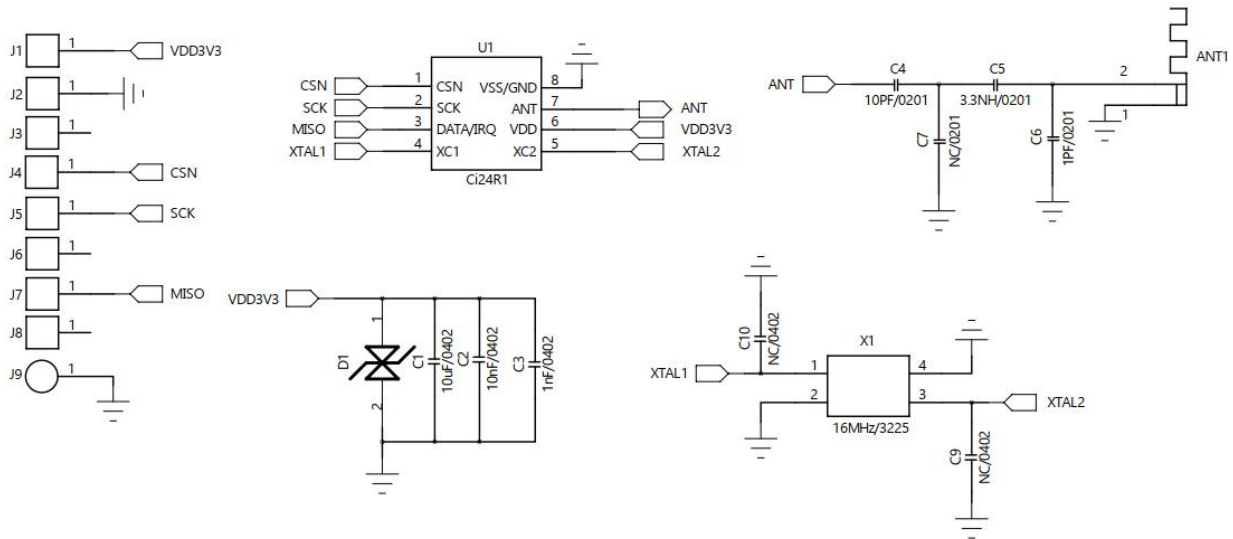


Figure 6 Schematic diagram of module

## 6. Antenna Parameter

### 6.1. Schematic diagram of antenna test prototype



Figure 7 schematic diagram of a simulated user welding a module to a motherboard

## 6.2. Antenna S parameters

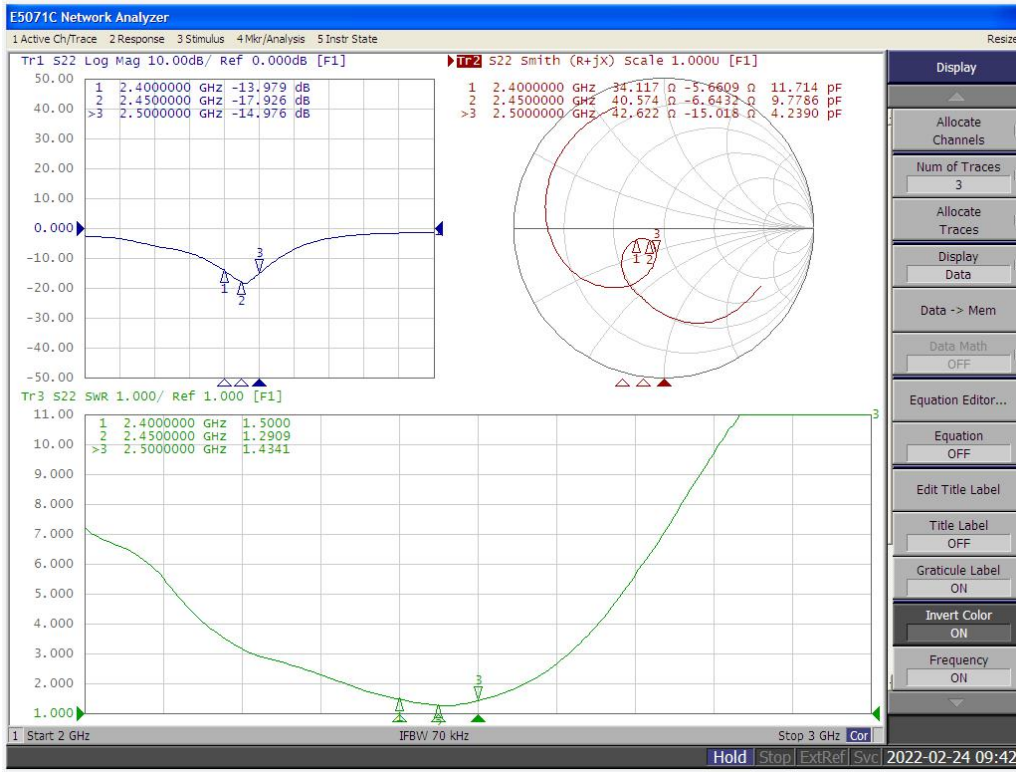


Figure 8 antenna S parameters

### 6.3. Antenna gain and efficiency

**Table 6 Antenna gain and efficiency**

Frequency ID	1	2	3	4	5	6	7	8	9	10	11
Frequency (MHz)	2400.0	2410.0	2420.0	2430.0	2440.0	2450.0	2460.0	2470.0	2480.0	2490.0	2500.0
Efficiency (dBi)	-3.03	-2.85	-2.84	-2.51	-2.85	-2.12	-2.16	-1.83	-1.79	-1.50	-1.70
Gain (dBi)	2.09	2.23	2.22	2.56	2.25	2.99	2.93	3.23	3.26	3.51	3.29
Efficiency (%)	49.80	51.84	51.94	56.14	51.90	61.34	60.80	65.62	66.28	70.80	67.55
Directivity (dB)	5.12	5.08	5.06	5.07	5.10	5.11	5.09	5.06	5.04	5.01	5.00
Peak Gain Position	165.00	165.00	165.00	165.00	165.00	165.00	165.00	165.00	165.00	165.00	165.00
Peak Gain Position	345.00	345.00	345.00	345.00	345.00	345.00	345.00	345.00	345.00	345.00	345.00
Efficiency ThetaPol	43.89	45.51	45.43	49.02	45.26	53.41	52.91	57.00	57.34	61.18	58.37
Efficiency PhiPol (%)	5.92	6.32	6.52	7.12	6.64	7.94	7.89	8.62	8.95	9.62	9.18
Upper Hem.	14.78	15.43	15.54	16.77	15.34	17.87	17.37	18.37	18.35	19.58	18.73
Lower Hem.	35.02	36.40	36.41	39.37	36.56	43.47	43.43	47.25	47.93	51.22	48.82

## 6.4. Antenna field pattern diagram

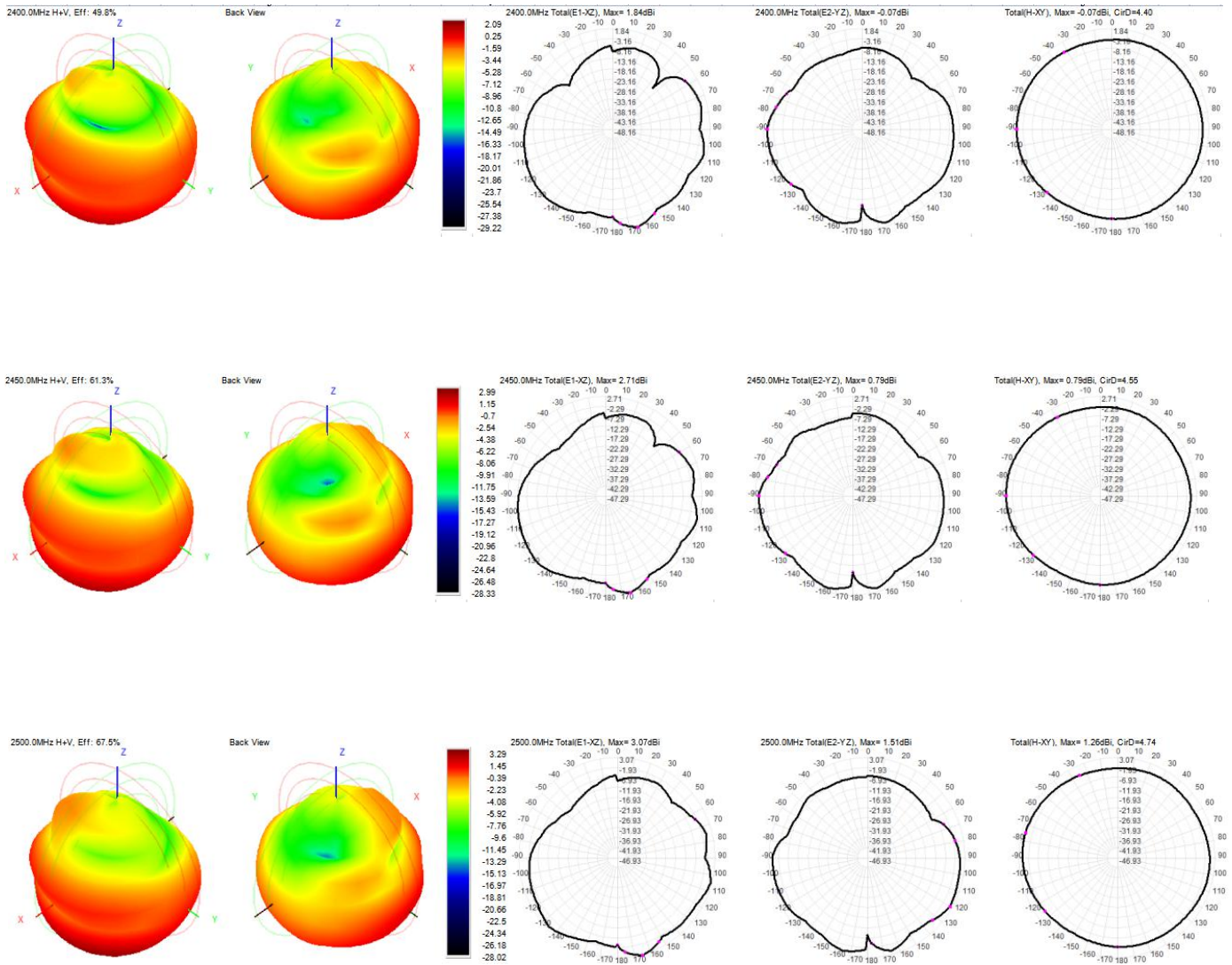


Figure9 Antenna field pattern diagram

## 7. Design guidance

### 7.1. Module application guide circuit

(>= 100mA, dC-DC or LDO independent power supply is recommended)

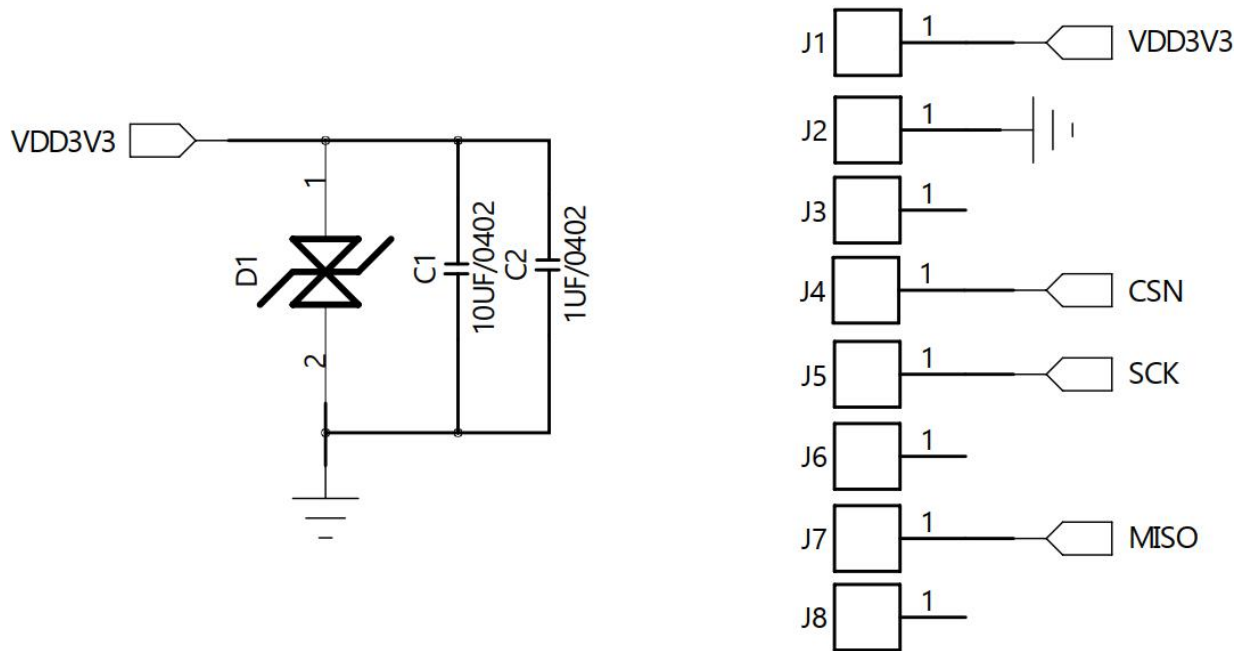


Figure 10 Application circuit diagram

### 7.2. Requirements for antenna layout

- The following two methods are recommended for the installation position on the mainboard:

Plan 1: put the module on the edge of the motherboard, and the antenna area extends out of the edge of the motherboard.

Plan2: put the module on the edge of the motherboard, the edge of the motherboard at the antenna position hollowed out an area.

- In order to meet the performance of onboard antenna, it is forbidden to place metal parts around the antenna and keep away from high frequency devices.



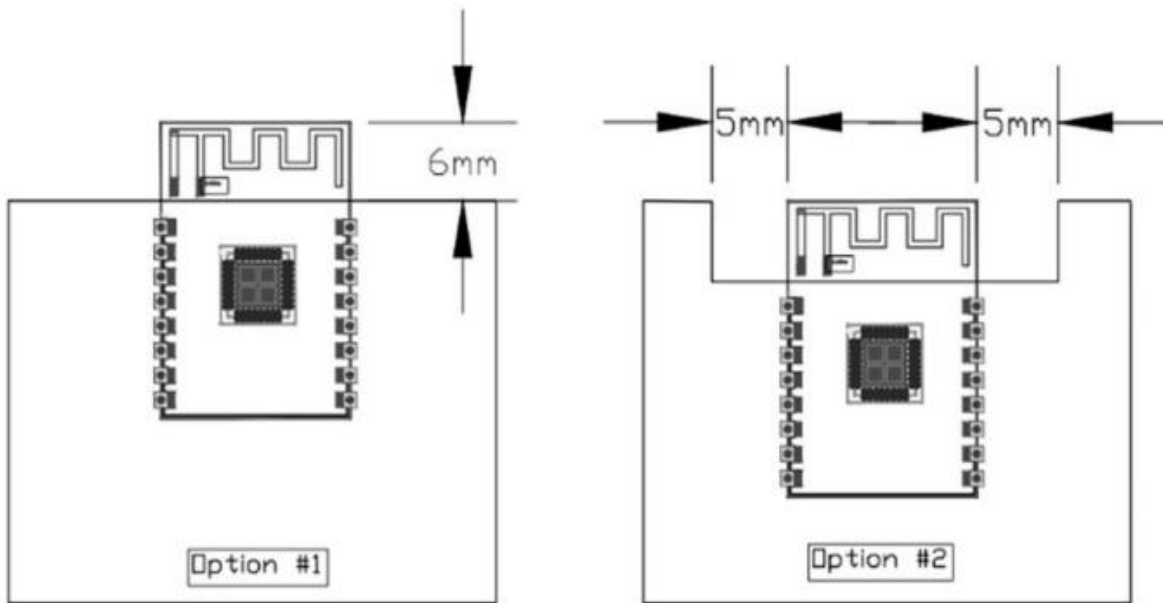


Figure 11 Antenna layout diagram

### 7.3. Power Supply

- 3.3V voltage and peak current above 100mA are recommended.
- LDO power supply is recommended; If the dc-dc is used, it is recommended that the ripple be controlled within 300mV under full load.
- It is recommended to reserve the location of the dynamic response capacitor for the DC-DC power supply circuit to optimize the output ripple when the load changes greatly.
- Electrostatic discharge (ESD) device is recommended for the 3.3V power port.

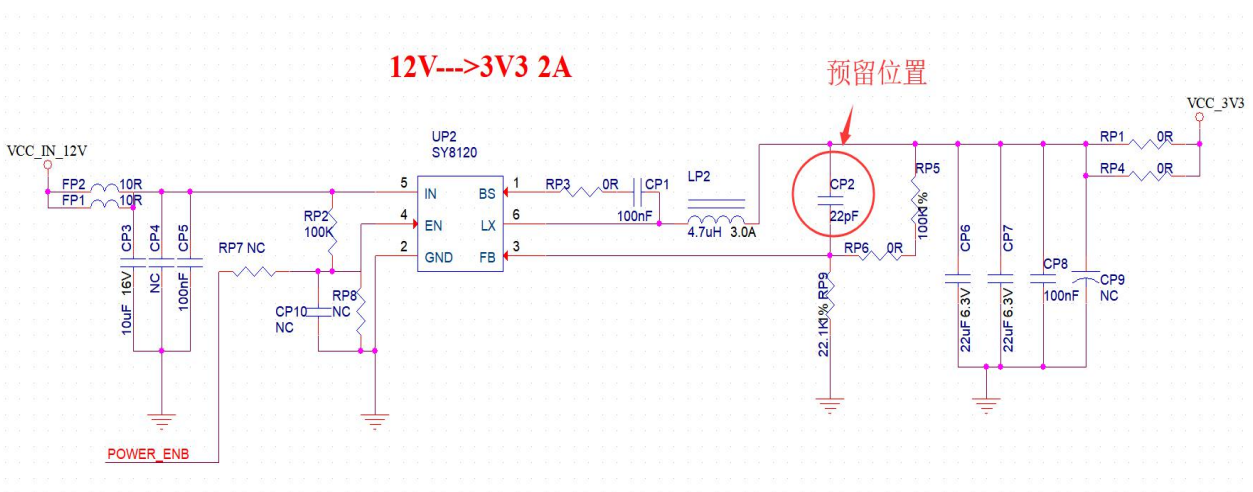


Figure 12 DC-DC buck circuit diagram

## 7.4. GPIO Level Switch

- The module leads out some IO ports. If necessary, it is recommended to connect the IO ports in series with a resistor of 10-100 ohm. This inhibits overshoot and makes both sides level more stable. It is helpful for EMI and ESD.
- For special I/O ports to be pulled up and down, refer to the usage instructions in the specifications, which may affect the module startup configuration.
- The IO port of the module is 3.3V. If the IO level of the main control and the module do not match, a level conversion circuit needs to be added.
- If the I/O port is directly connected to a peripheral port or a pin row terminal, you are advised to reserve an ESD device near the terminal where the I/O port is routed.

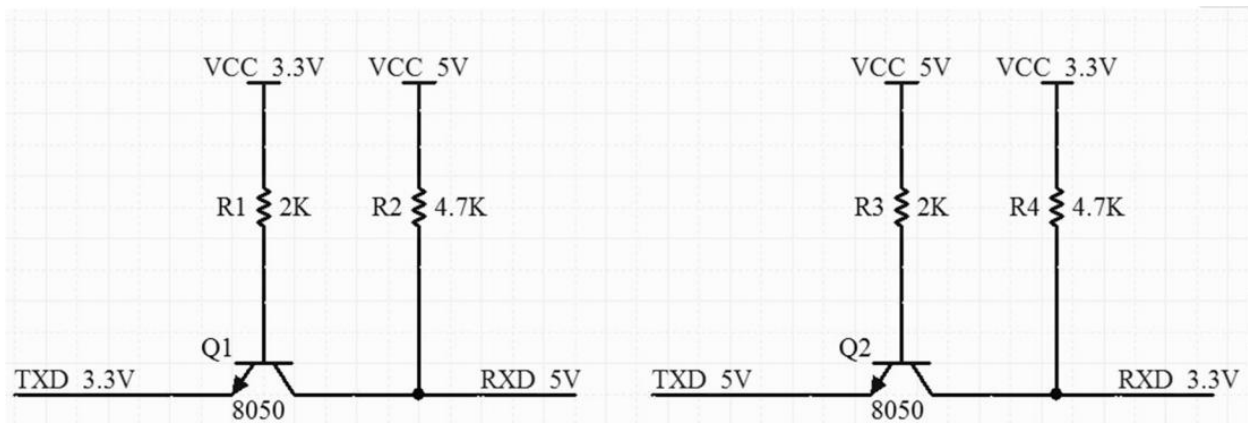


Figure 13 Level switching circuit

## 8. Reflow Soldering Curve

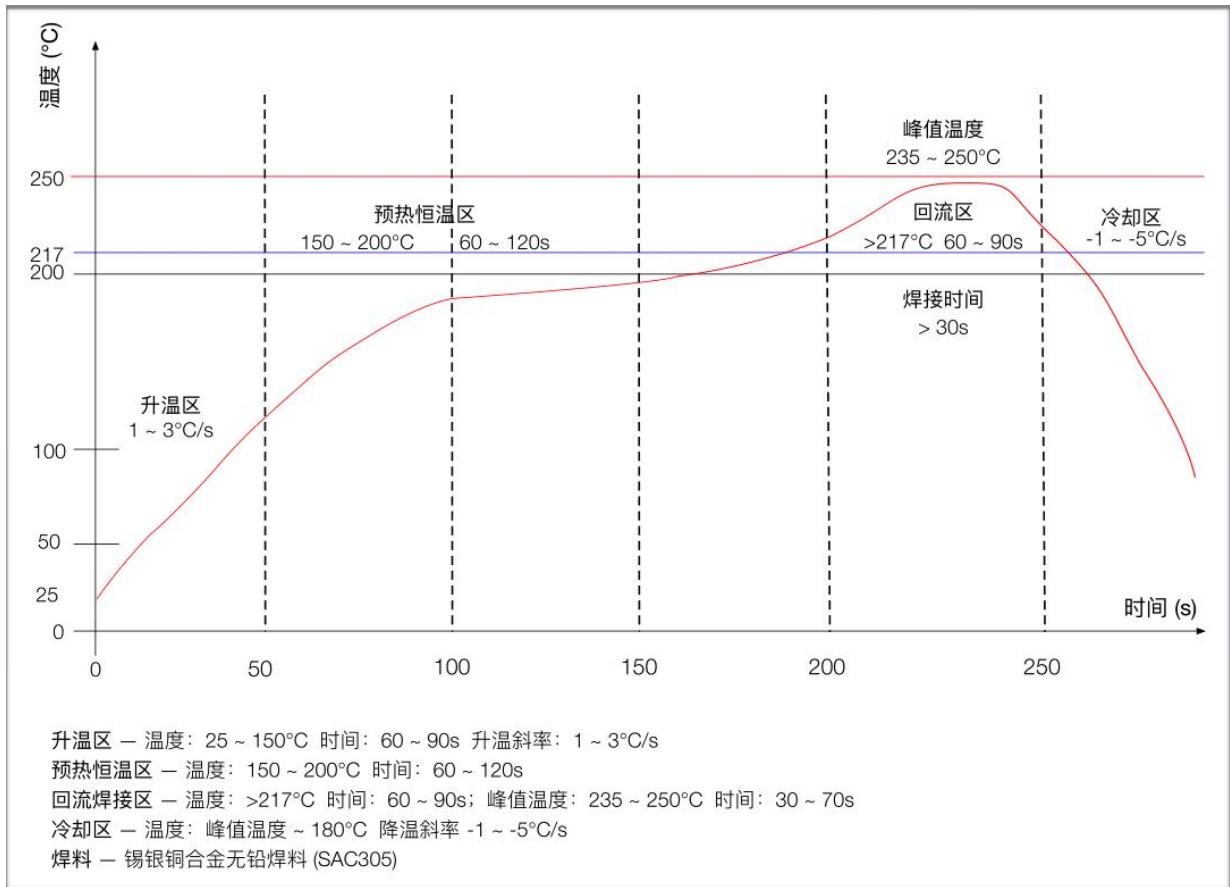


Figure 14 Reflow soldering curve diagram

## 9. Product Related Model

Table 7 Product model table

Product model	Power supply	Package	Size	Antenna interface
NF-05	2.1V ~ 3.6V, I>100mA	SMD-8	12.0*18.0*0.8( ±0.2)mm	On board PCB antenna
NF-05-S	2.1V ~ 3.6V, I>100mA	DIP-8	28.6*15.2*12( ±0.2)mm	On board PCB antenna

Product related information: <https://docs.ai-thinker.com>

## 10. Product Packaging Information

NF-05 module is packed with braided tape, 1600PCS/reel. As shown below:



Figure 15 Packing tape drawing

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[Tmall shop](#)

[Taobao shop](#)

[Alibaba shop](#)

[Technical support email: support@aithinker.com](mailto:support@aithinker.com)

[Domestic business cooperation: sales@aithinker.com](mailto:sales@aithinker.com)

[Overseas business cooperation: overseas@aithinker.com](mailto:overseas@aithinker.com)

Company Address: Room 403,408-410, Block C, Huafeng Smart Innovation Port, Gushu 2nd Road, Xixiang, Baoan District, Shenzhen.

Tel: +86-0755-29162996



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